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# LCFC Confidential

## BETTA MB Schematics Document

Alder Lake-U CPU with DDR4 + Slot-DIMM

2022-03-19

REV: 0.1

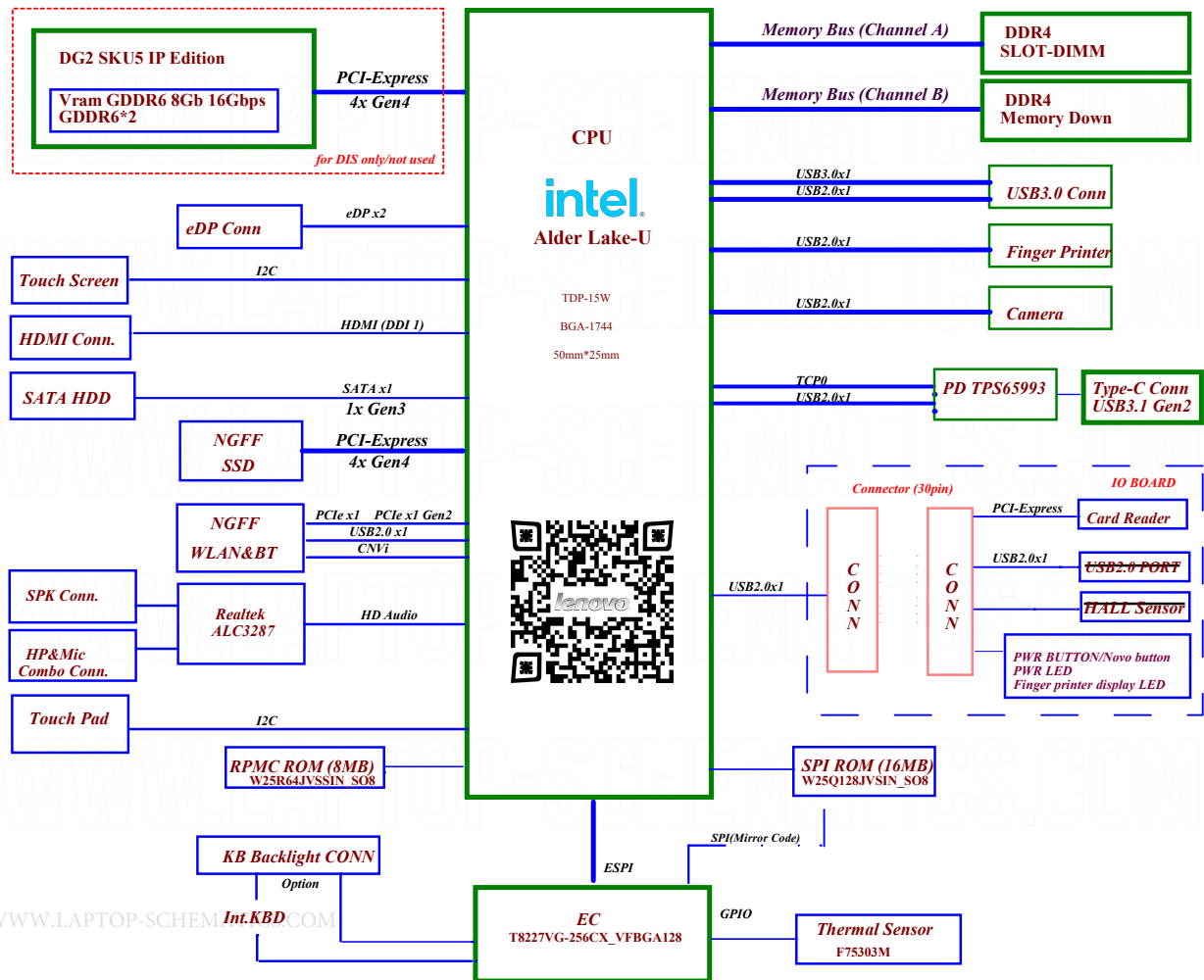
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## Betta\_ADL-U Block Diagram

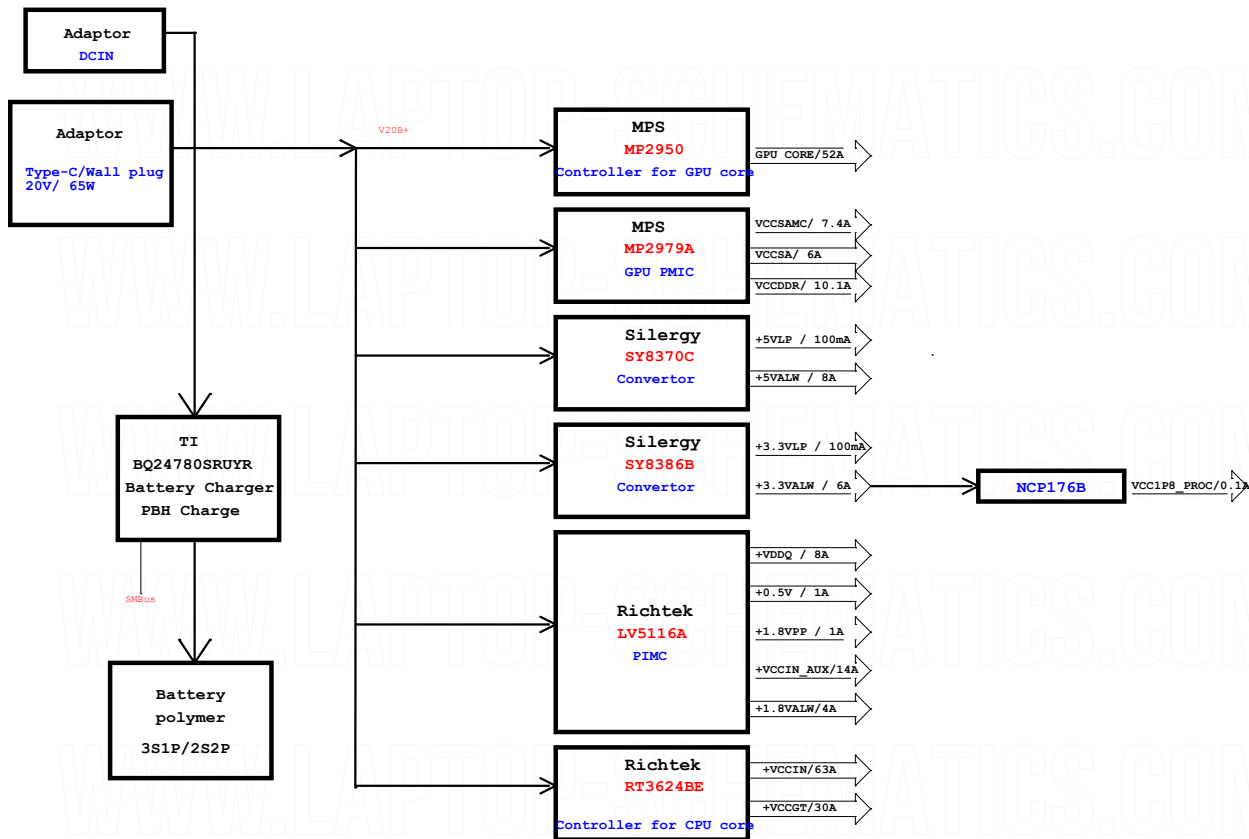


## Project : Betta

PCB # JS476&amp;JS576 NM-E331

I/O BD # JS476 NS-E331 (for 14") / JS576 NS-E332 (for 15")

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SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALN	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

### SMBUS Control Table

EC SMBus1_address		EC SMBus2_address		EC SMBus3_address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT771BW)	1001_100b	not use		DDR4 SODIMM	need to update
Charger	0001 0010 b	PCH	need to update			WLAN	Reserved
U-PWR Controller	need to update					DGPU	need to update

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								C	Notes For VGA	0.1
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BOM Structure	Description
@	Un-stuff
FHD@	For FHD Panel Part
HDR@	For HDR Panel Part
14@	For 14" part
15@	For 15" Part
17@	For 17" Part
8M_ROM@	For 8G B108 ROM part
AMP@	For external Amplifier solution part
AMP_NS@	For external Amplifier solution un-stuff part
AMP_PWR@	For discrete Amplifier power solution part
ANS@	For power ANS solution part
USM@	For power USM solution part
BL@	For Key Board Backlight part
CD@	For C cost down
CHANNELA@	For Memory Channel A part
DDPA@	For Memory Channel A DOP part
SDPA@	For Memory Channel A SDP part
DDPB@	For Memory Channel B DOP part
SDPB@	For Memory Channel B SDP part
NPI@	For NPI Phase part
MP@	For MP Phase Part
PCIE4@	For PCIE Gen4 part
EMC@	For EMC part
EMC 15@	For GY051 EMC part
EMC_NS@	For EMC un-stuff part
RF_NS@	For RF Un-stuff part
AOAC@	For AOAC part
CNVI@	For CNVI WLAN part
ME@	For ME part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For Touch Pad Part
UMA@	For UMA part

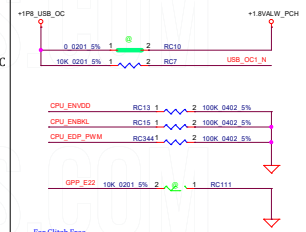
PCB	
CPU	
DRAM /Board ID	<p>See page # 11</p>

See page # 11

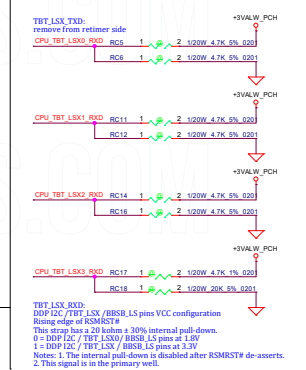
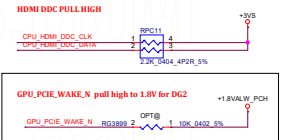
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			<small>NOT</small>	<small>Revised Name</small> <b>Notes For ECM</b>	<small>1</small>
			<small>LCFC</small>		

# Design Notice

USB3/USB2 Port Pairing for USB-C Connectors				
	TC09	TC11	TC12	TC13
CPU USB3 port#	1	2	3	4
PCI USB2 port#	2	3	4	6

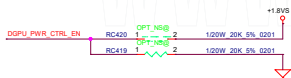


For Glitch Free  
Cap or pull-down resistor is required depending on panel power sequencing step or power delivery  
Option 1:Cap Implementation  
330 nF for 2.4V Ramp Rate from 5-50ms  
33 nF for 3.3V Ramp Rate Less than 5ms  
Option 2:Pull-down Resistor Implementation  
100K for 3.3V Signaling Mode  
75K for 1.8V Signaling Mode

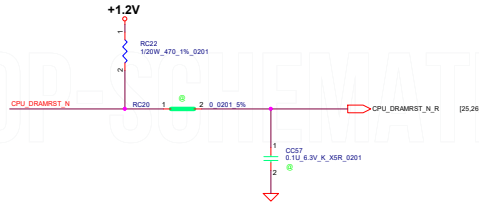
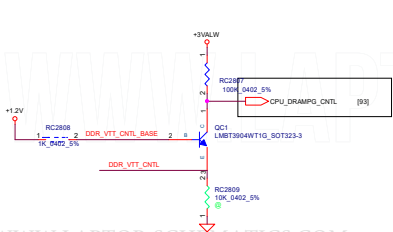
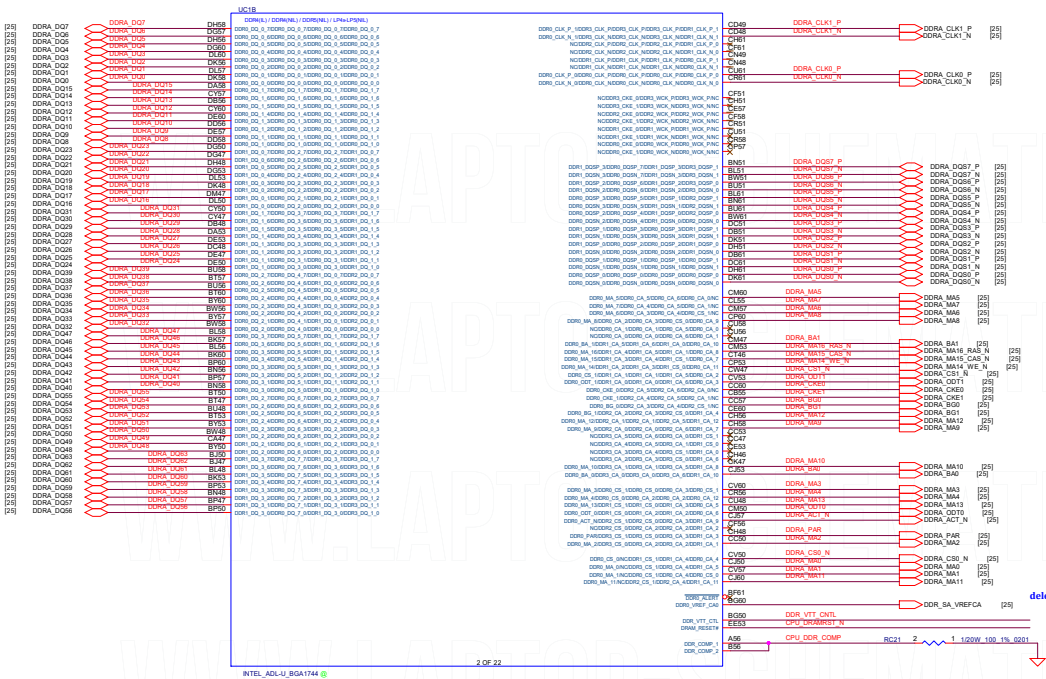


TBT\_L5X\_TXD:  
remove from retimer side  
CPU TBT\_L5X1\_RXD: RC11 1 2 1/20W 4.7K 5% 0201  
CPU TBT\_L5X1\_RXD: RC12 1 2 1/20W 4.7K 5% 0201  
CPU TBT\_L5X2\_RXD: RC14 1 2 1/20W 4.7K 5% 0201  
CPU TBT\_L5X2\_RXD: RC16 1 2 1/20W 4.7K 5% 0201  
CPU TBT\_L5X3\_RXD: RC17 1 2 1/20W 4.7K 5% 0201  
CPU TBT\_L5X3\_RXD: RC18 1 2 1/20W 20K 5% 0201  
TBT\_L5X\_RXD:  
DDP\_L2C / TBT\_L5X / BBSR\_L5 pins VCC configuration  
Rising edge of RSMRST#  
This strap has a 20 kohm + 30% internal pull-down.  
0 = DDP\_L2C / TBT\_L5X0 / BBSR\_L5 pins at 3.3V  
1 = DDP\_L2C / TBT\_L5X / BBSR\_L5 pins at 1.8V  
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.  
2. This signal is in the primary well.

the diffrent with Base:  
1.C970 Use TCP for TBT,S170 no USE  
2.C970 Use GPP\_E18&E20,S170 no USE  
3.C970 Stuff RC12,RC6,RC16,S170----- @  
4.C970 No HDMI CONN,S170 have



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				P007-CPU (1/16) : (DDI/EDP/TBT)	1.0
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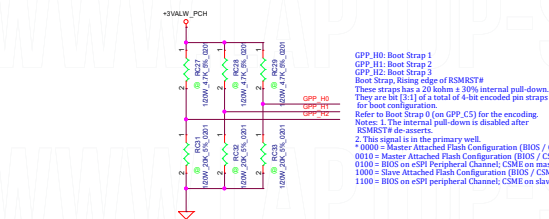
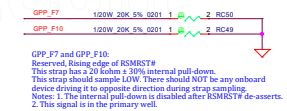
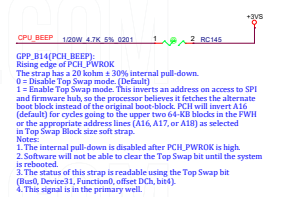
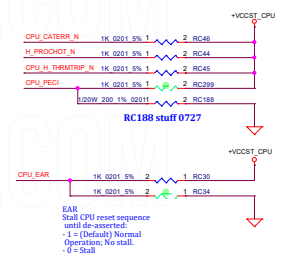
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C		P008-CPU (2/16) : (LPDDR4X-CH)		P008-CPU (2/16) : (LPDDR4X-CH)		1	
Date		March 10, 2022		Sheet		8 of 118	




CPU_JTAG_TCK	0	0.0201	5%	1		2	RC48	POH_JTAG_JTAGX
CPU_JTAG_TRST	N	0.0201	5%	1		2	RC60	POH_JTAG_TRST_N
CPU_JTAG_TMS	0	0.0201	5%	1		2	RC23	POH_JTAG_TMS
CPU_JTAG_TDO	0	0.0201	5%	1		2	RC24	POH_JTAG_TDO
CPU_JTAG_TDI	0	0.0201	5%	1		2	RC62	POH_JTAG_TDI

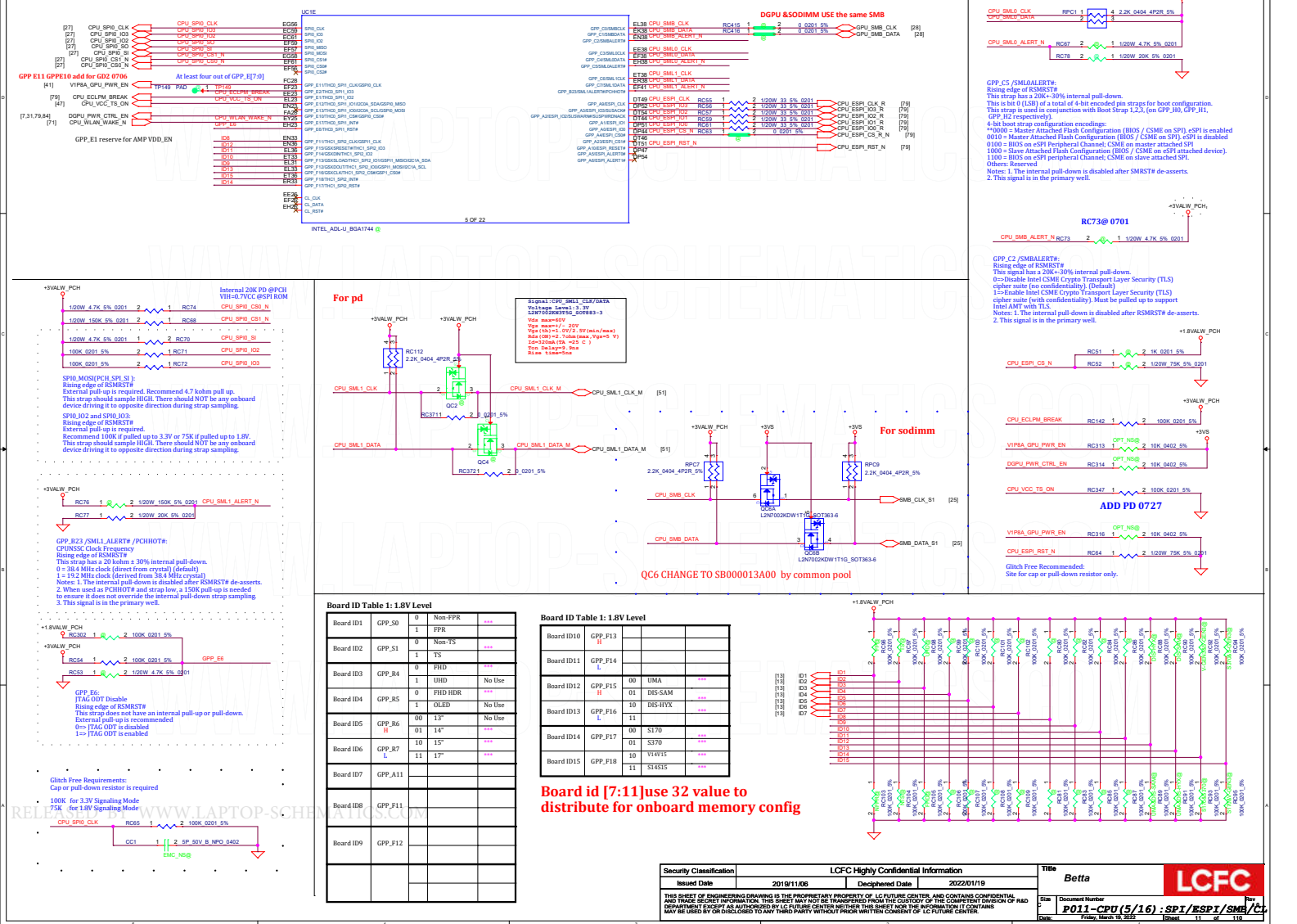
EC SCI N 10K 0201 5% 1 2 RC47 +3VS

**DELETE ISH RC308 PULL HIGH TO 3VS RSVD**



**EMC REQUIRED 0624**

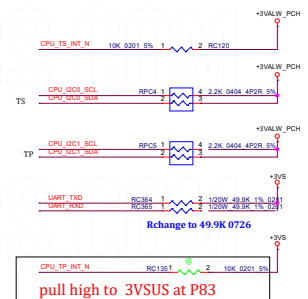
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		P010-CPD(4/16)		MISC		JTJG	
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## Design Notice

S170 have not TOF and AMP  
 remove RC129 RC130 pull high to +3VS  
 remove RC269,RC270 pull high to +3VS  
 remove RC306,RC307 pull high to +3VS  
 remove RC272,RC124,RC127,RC128 pull high to +3VS  
 remove RC27 pull high to +3VALW\_PCH  
 remove RC141 pull high to +3VALW\_PCH

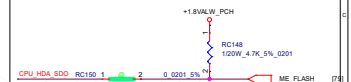
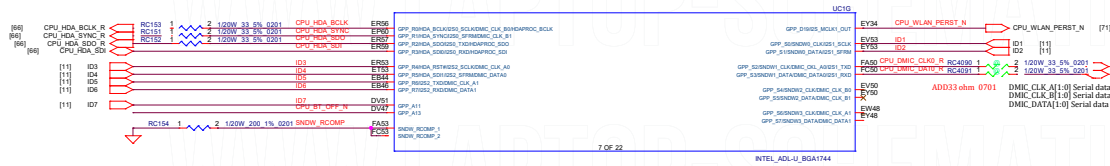


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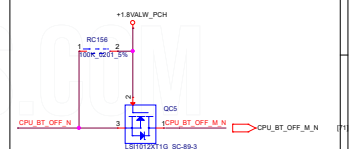
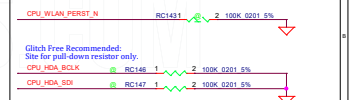
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				1	P012-CPU(6/16: T2C/ISH/UART/GP10
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## Design Notice

pay attention to this id3,  
connect to the unused id better

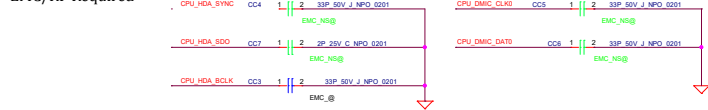


GP2 (PCH\_HDA\_SDO):  
Flash Descriptor Security Override  
Rising edge of PCH\_PWRON  
This strap has a 20 kOhm ± 30% internal pull-down.  
0 => Enable security measures defined in the Flash Descriptor (Default)  
1 => Disable Flash Descriptor Security (override) This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.  
Notes: 1. The internal pull-down is disabled after PCH\_PWRON is high.  
2. This signal is in the primary well.



Signal: CPU\_BT\_OFF\_M\_N  
Voltage: 1.1V  
LSI1012X110\_SC-69-3  
Vda max=25V  
Vda min=1.1V  
Vda (oh)=0.45V/0.9V (min/max)  
Rda (oh)=1.1kOhm/1.1kOhm, Vpart=4V  
Zin Delay=50ns  
Rise Time=100ns

## EMC/RF Required



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1.S170 CARD READER USE PCIE4 BUS  
2.S170 SSD USE PCIE4 BUS



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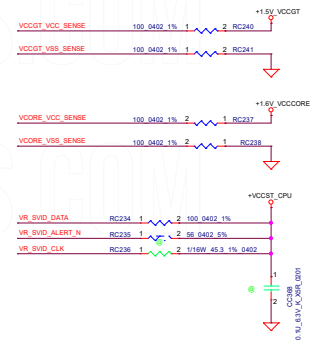
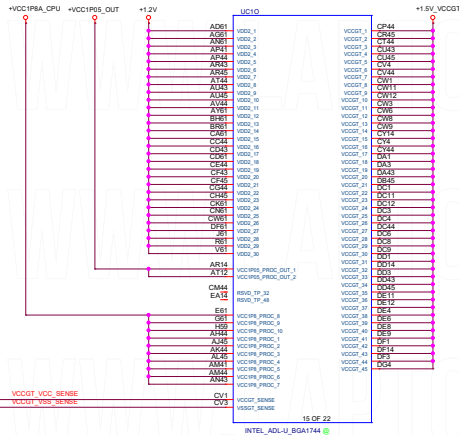
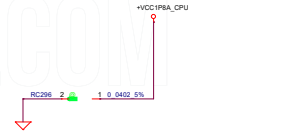
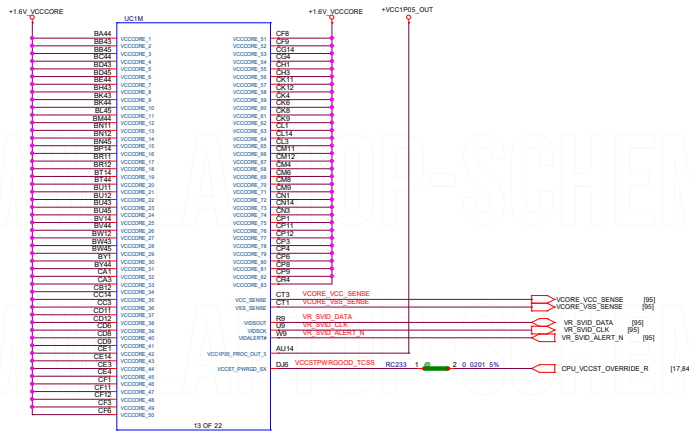
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## EMC/RF Required



## 1.5VCCGT ADD RF C?

Place as close as possible to the package (less than 3mm).

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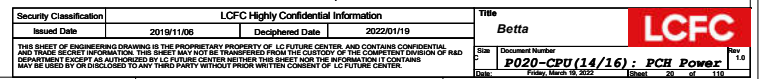
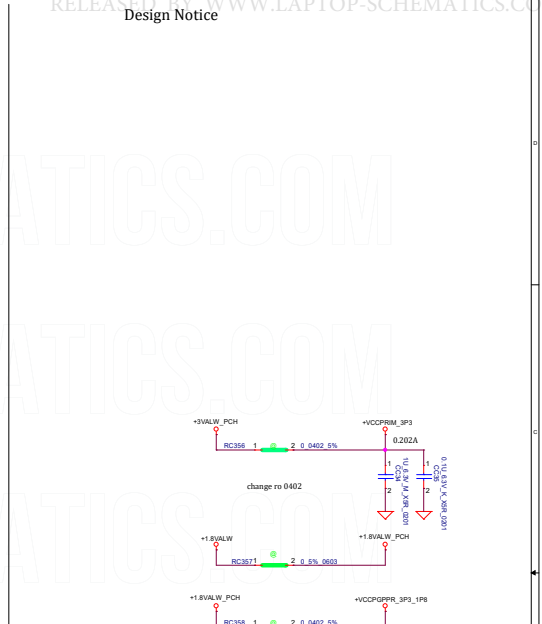
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UCID	
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AL25	REV0, 5
AL25	REV0, 7
BO25	REV0, 8
BO25	REV0, 9
DT25	REV0, 10
DT25	REV0, 13
EE25	REV0, 15
EP25	REV0, 16
EH21	REV0, 20
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				1/8"	P022-PCB PWR Reserved
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				Sheet	22 of 118

## CFG STRAPS for CPU

Reserved configuration lane	
CFG[1:0]	N/A
PCI Express® Static x8 Lanes Numbering Reversal	
CFG2	1 = Normal operation ★ 0 = Lane numbers reversed.
Reserved configuration lane	
CFG3	N/A
Reserved	
CFG4	N/A
PCI Express® Bifurcation	
CFG[6:5]	N/A
Reserved configuration lane	
CFG[13:7]	N/A
PEG6 Lane Reversal	
CFG14	★ 1 = (default) normal 0 = Reversed
PEG6 Lane Reversal	
CFG15	★ 1 = (default) normal 0 = Reversed
Reserved configuration lane	
CFG[17:16]	N/A

Signal Name Description  
Vss Ground Processor ground node  
Vss\_NCTP Non-Critical To Function: These signals are for package mechanical reliability and should not be connected on the board.  
RSVD Reserved: All signals that are RSVD should not be connected on the board.  
RSVD\_NCTP Reserved Non-Critical To Function: RSVD\_NCTP should not be connected on the board.  
RSVD\_TP Test Point: Intel recommends to route each RSVD\_TP to an accessible test point. Intel may require these test points for platform specific debug. Leaving these test points inaccessible could delay debug by Intel.

★ GPP\_B18\_NO\_REBOOT  
0 = Disable No Reboot mode (Default)  
1 = Enable No Reboot mode (PCI will disable the timer system reboot feature). This function is useful when running ITT/IOV  
RC255 1K\_0402\_5% Place near PC4  
GPP\_B18\_NO\_REBOOT

PDG page319

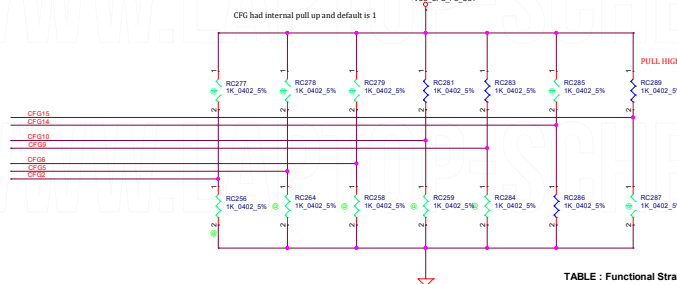
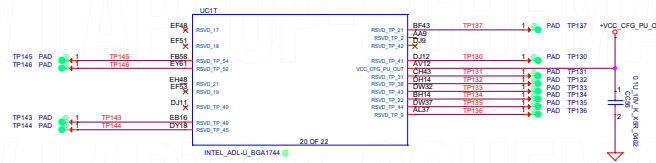
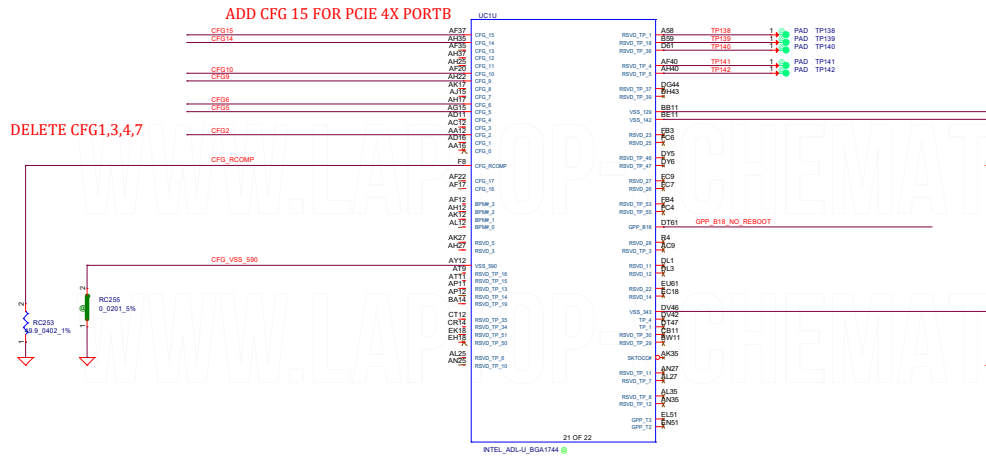


TABLE : Functional Strap

GPP_B18/GSP10_MOSI (No Reboot)	R563
HIGH Enable "No Reboot" Mode	ASM
LOW Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

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				Issue	Sheet 22 of 118

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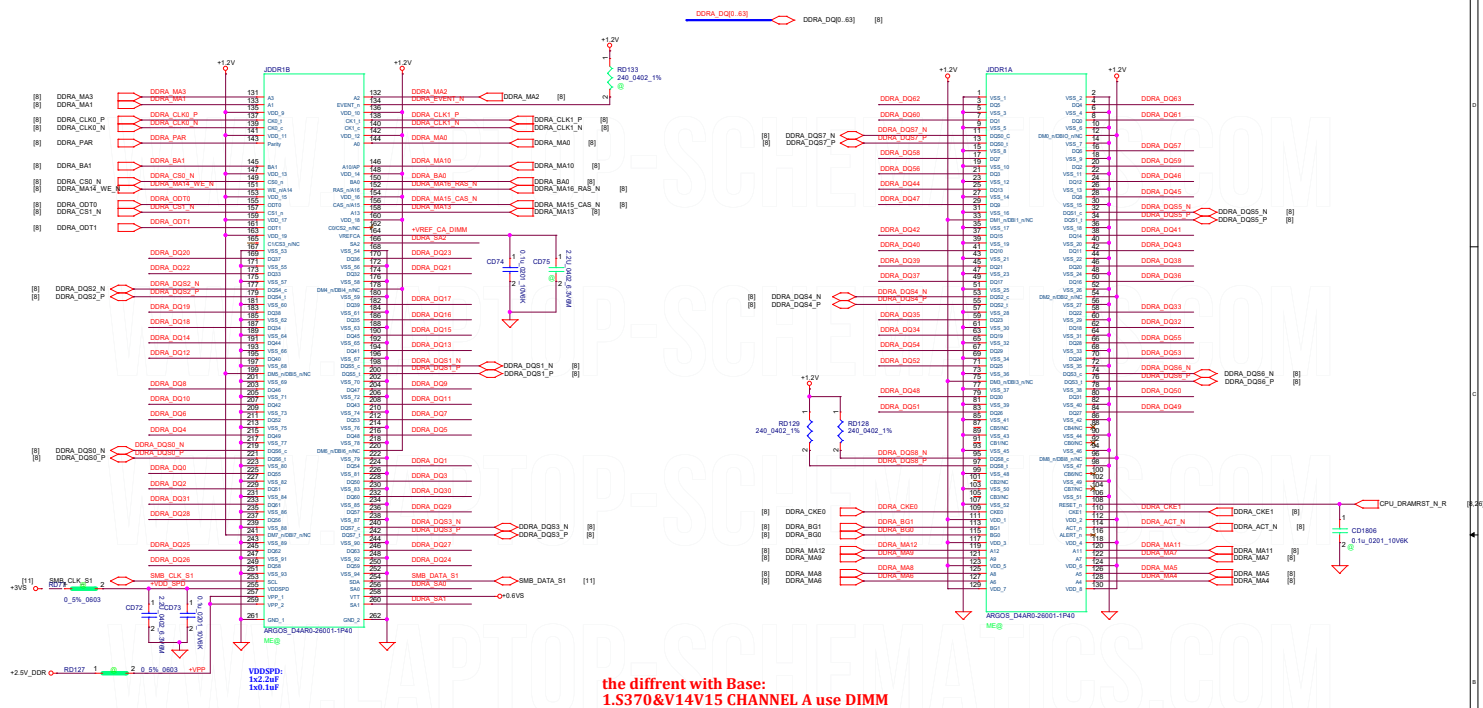
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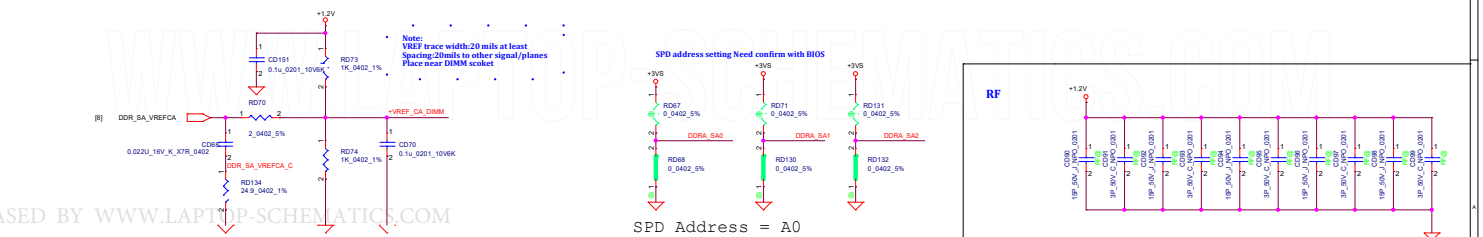
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P024-STEP-00A					1



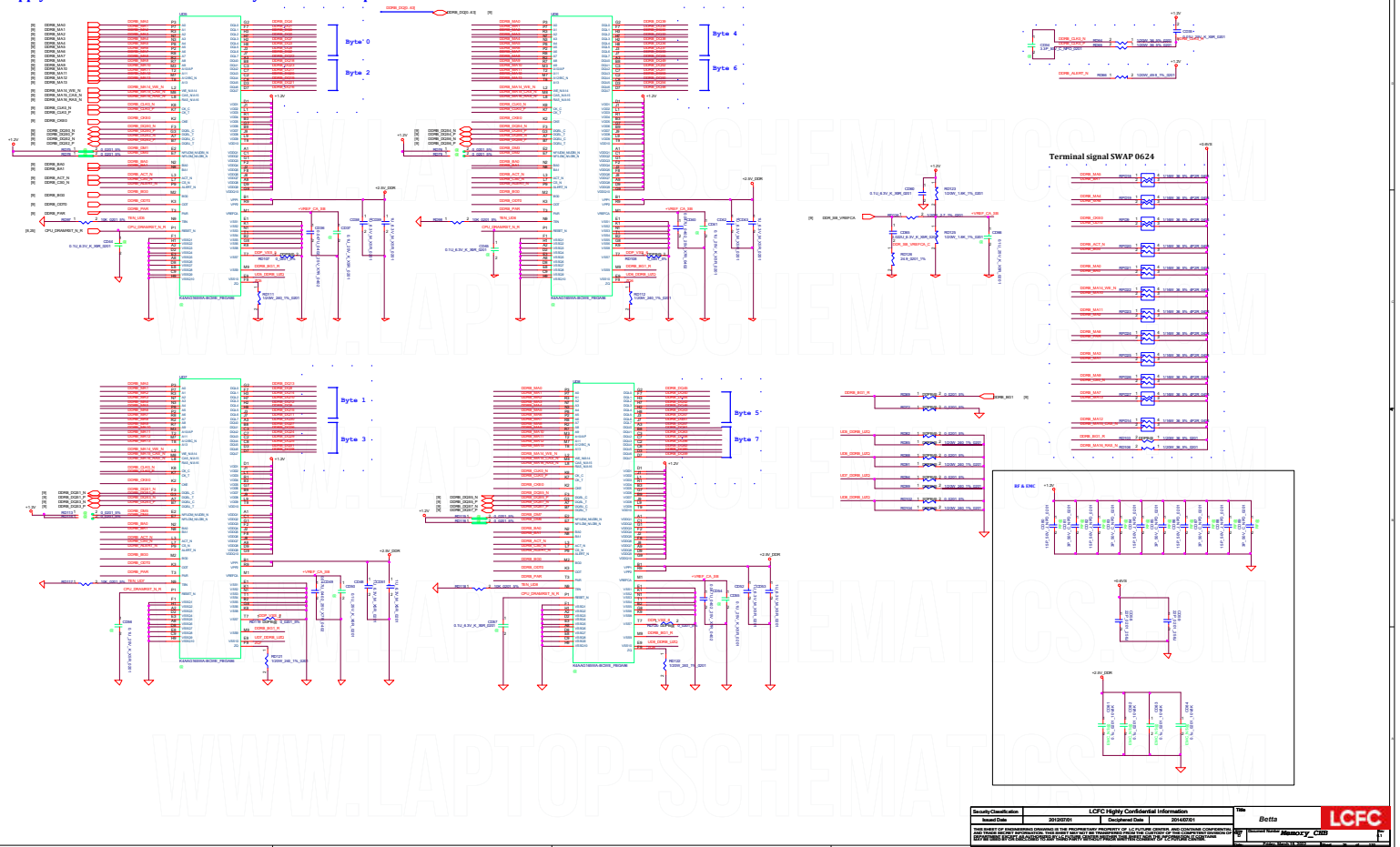
the diffrent with Base:  
1.S370&V14V15 CHANNEL A use DIMM



SPD Address = A0

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Title	Beta		
Doc Number	Memory_CHA		
Date	Friday, March 16, 2012	Sheet	25 of 118

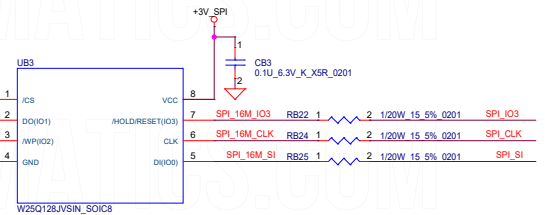
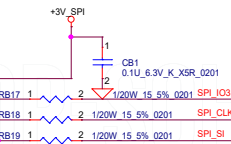
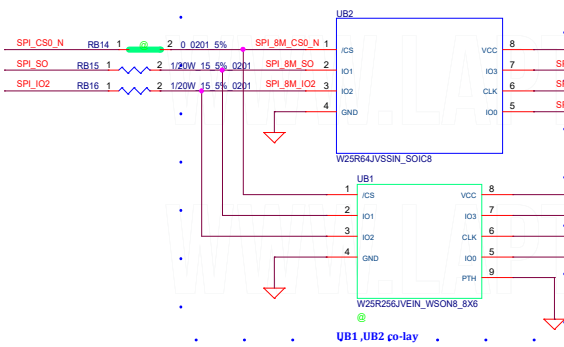
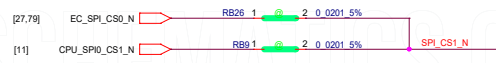
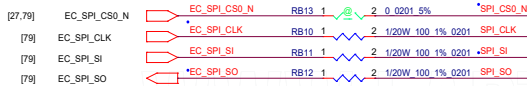
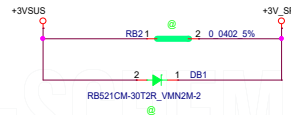
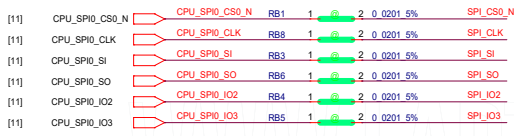
## Apply X76 BOM to control SDP Memory Stuff components!



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RB3,4,5,6,8CHANGE TO 00HM



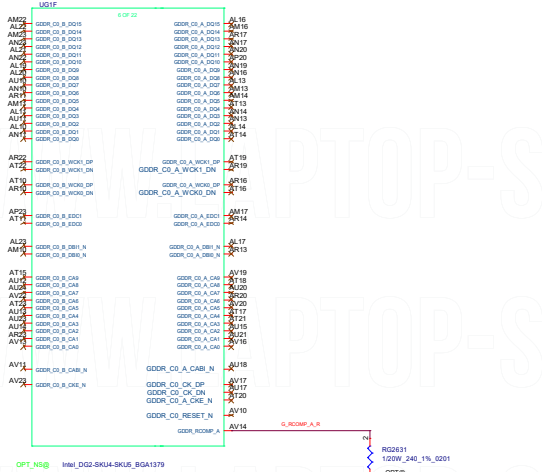
UB2 UB3 are changed FROM IQ to IN by common pool

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				Size	Document Number
				B	SPI ROM/TPM
				Date	Friday, March 19, 2022
				Sheet	27 of 110

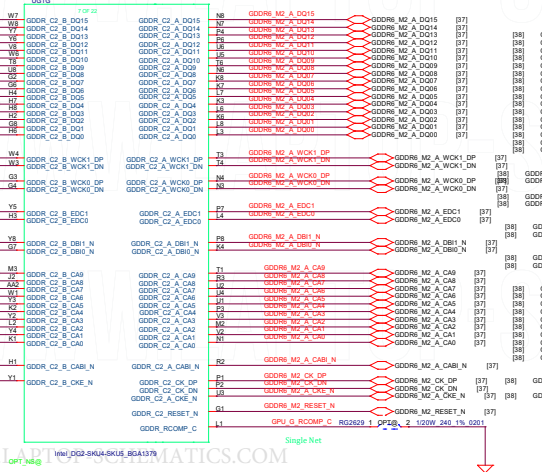
## PCIE INTERFACE X4



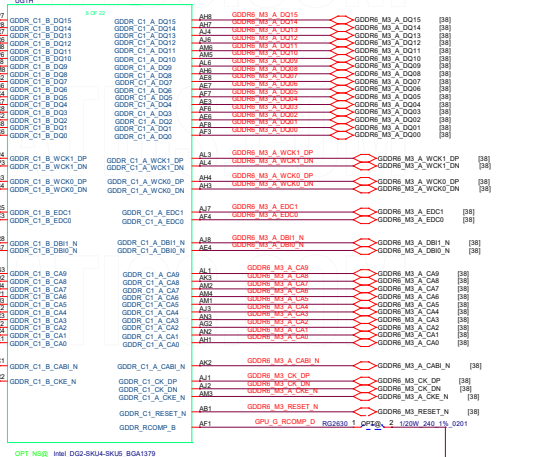
# GPU GDDR6 CHANNELS M1



# GPU GDDR6 CHANNELS M2



# GPU GDDR6 CHANNELS M3




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Size	Document Number					Rev	
	P030-GPU MRM Interface (A/B)					1.0	
Date	Friday, March 15, 2012					Sheet 30 of 113	

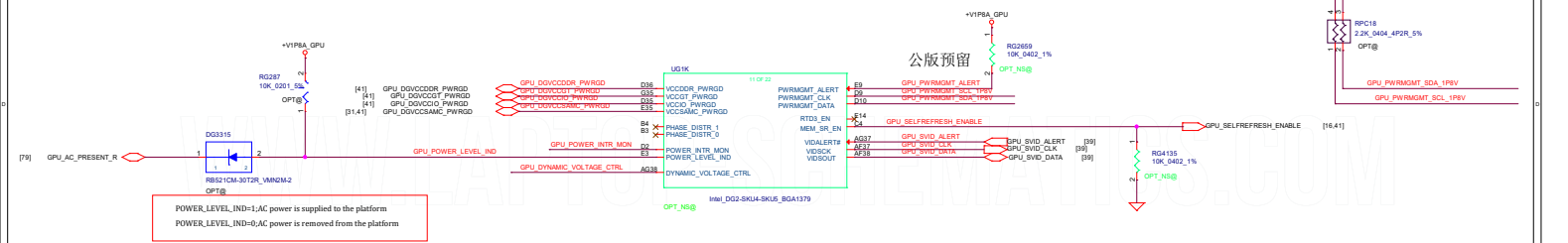
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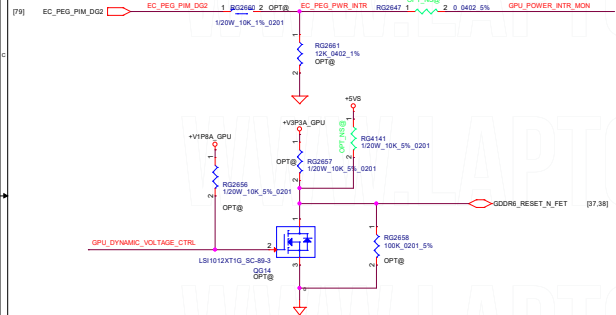
**EMC REQUIRED 0624**

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Date	Friday, March 10, 2022		Sheet	1 of 113	

GPU: GPIO 1 AND 2



NEED CONNECTED TO EC GPIO



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					Document Number <b>P032-GPU GPIO/JTAG</b>
					Rev 1.0
					File: P032_GPU_GPIO_JTAG
					Sheet 92 of 113

DEBUG

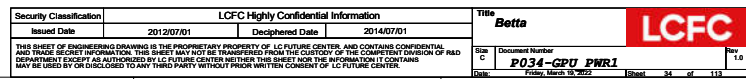
RSVD

BOARD IDENTIFICATION FOR DG2 FIRMWARE

GPU DDI: A,C,D

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				P033-GPU Strap	1.0
				Issue	138

## +V1P8A\_PLLVPH\_GPU



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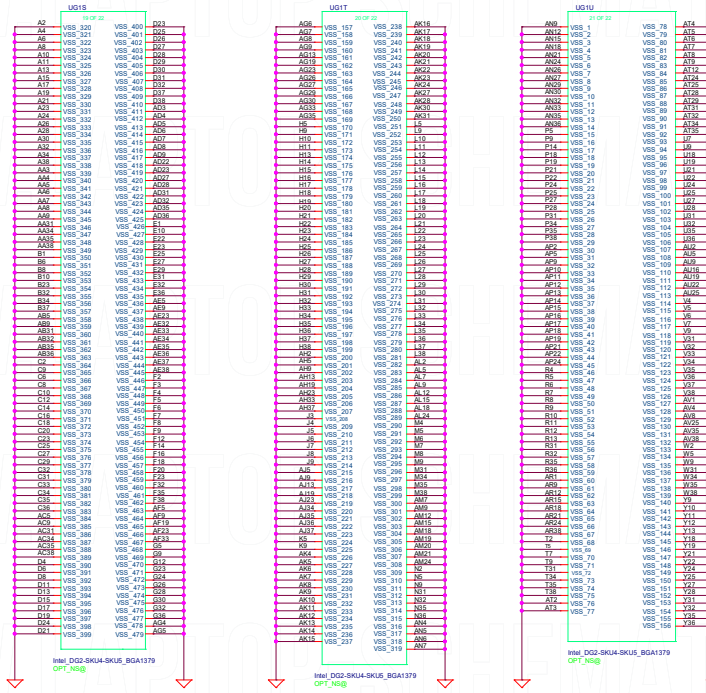
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Title		P035, March 10, 2012		Sheet		35		of 113	

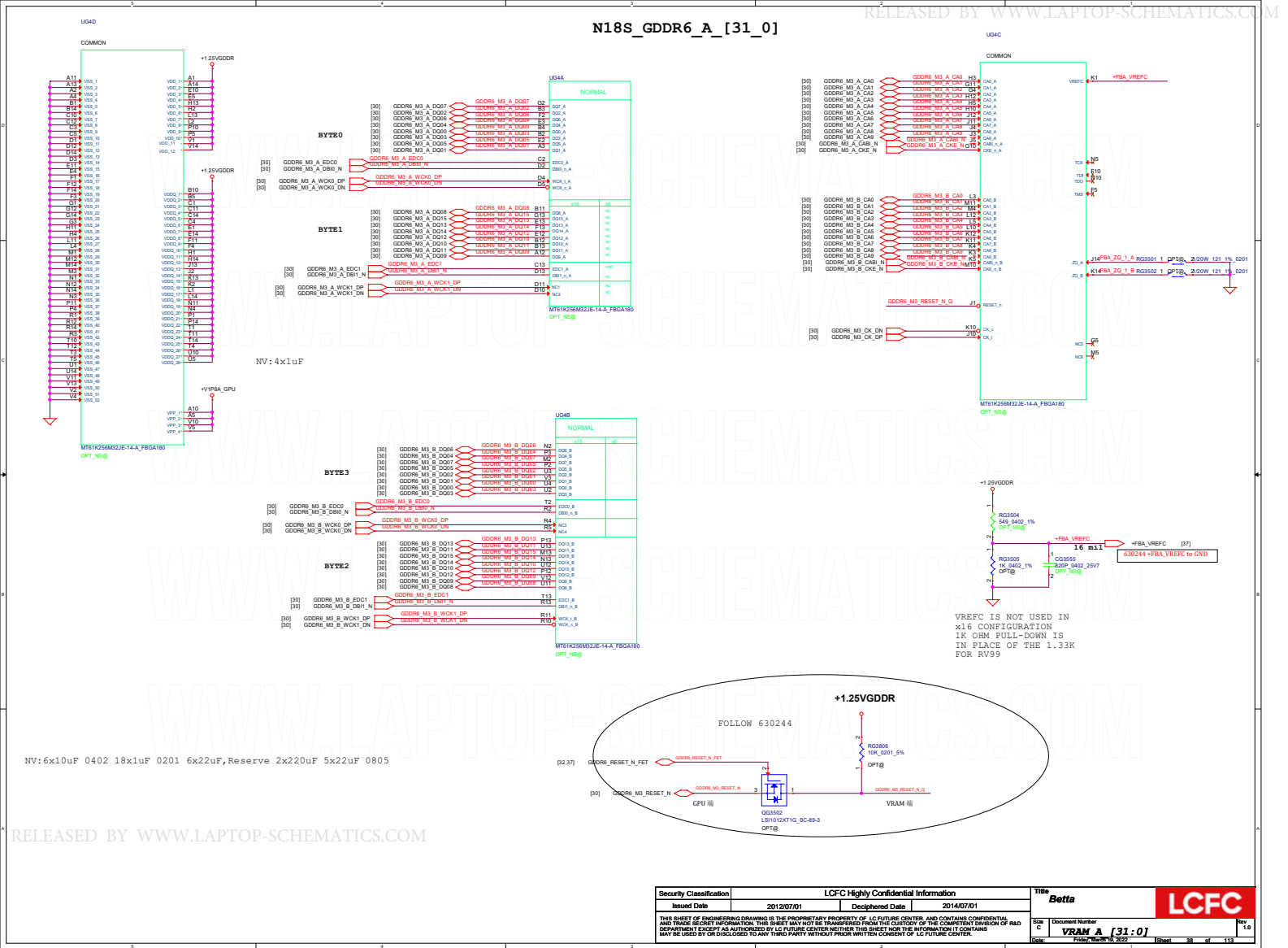
# GPU POWER: GROUND



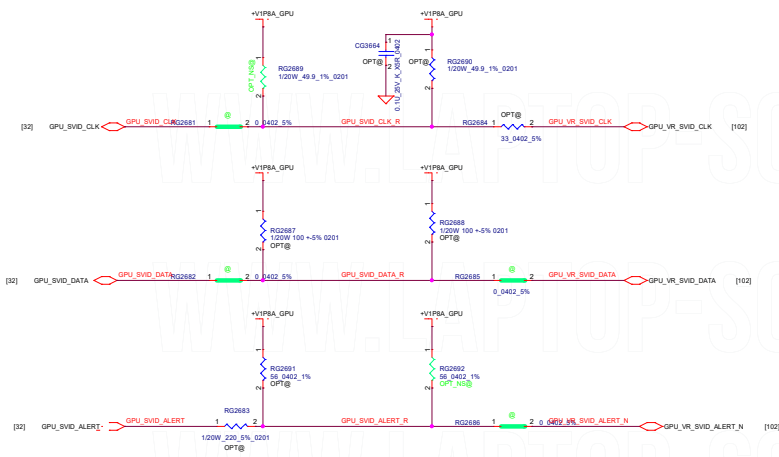
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Title		P036, March 10, 2012		Sheet	36 of 113



# N18S\_GDDR6\_A\_[31\_0]

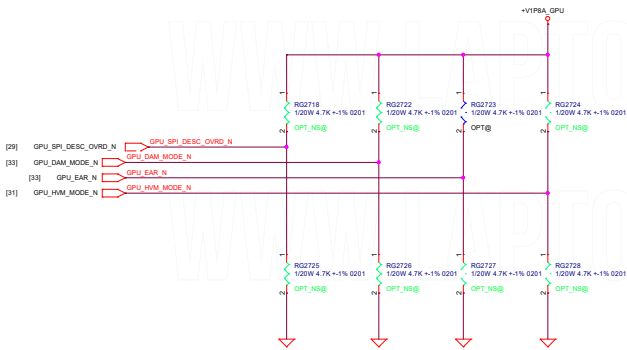
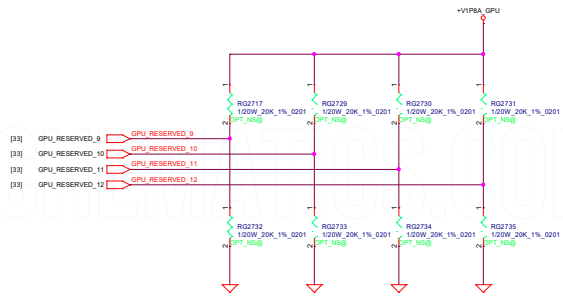


## GPU VREG: SVID



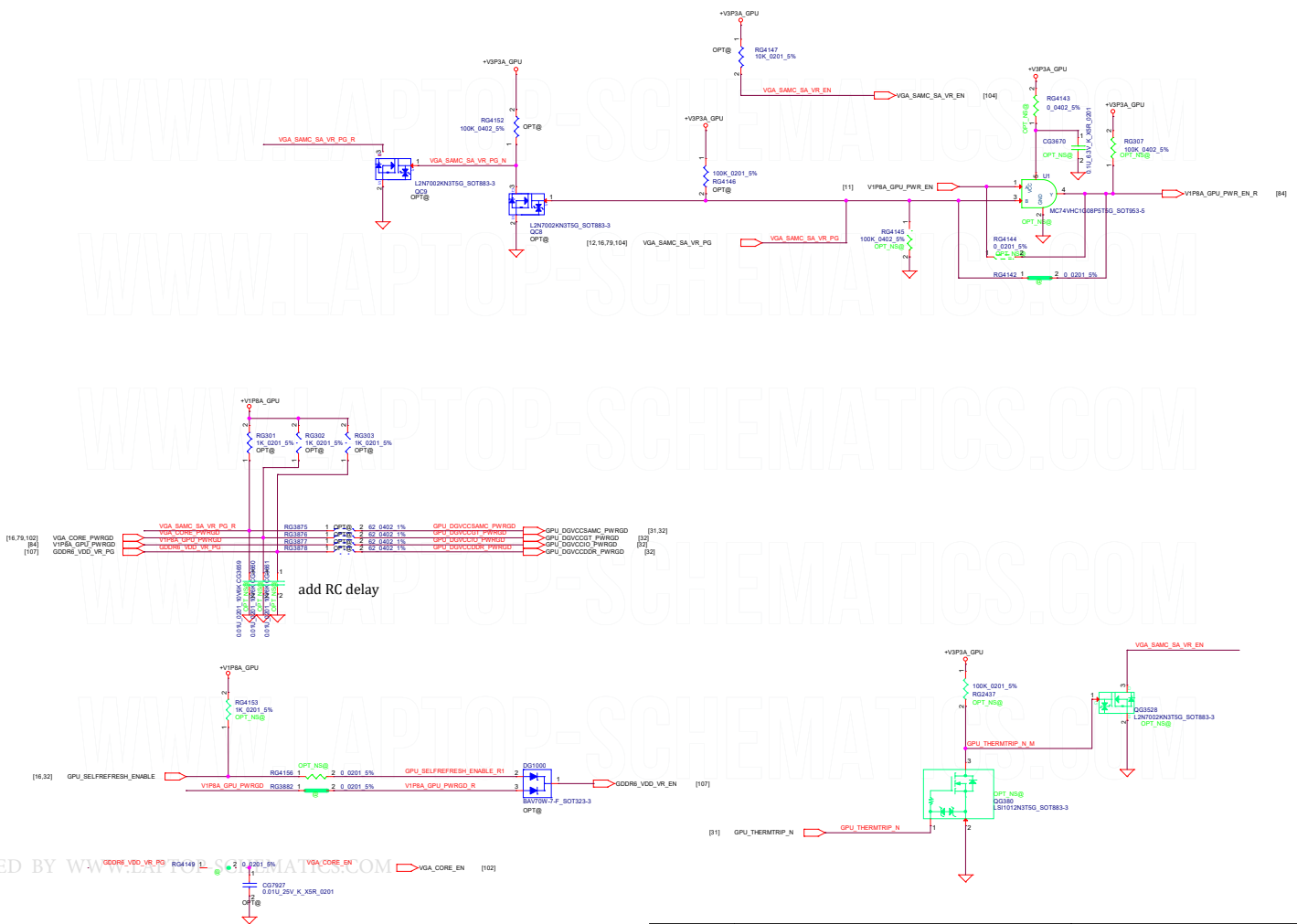
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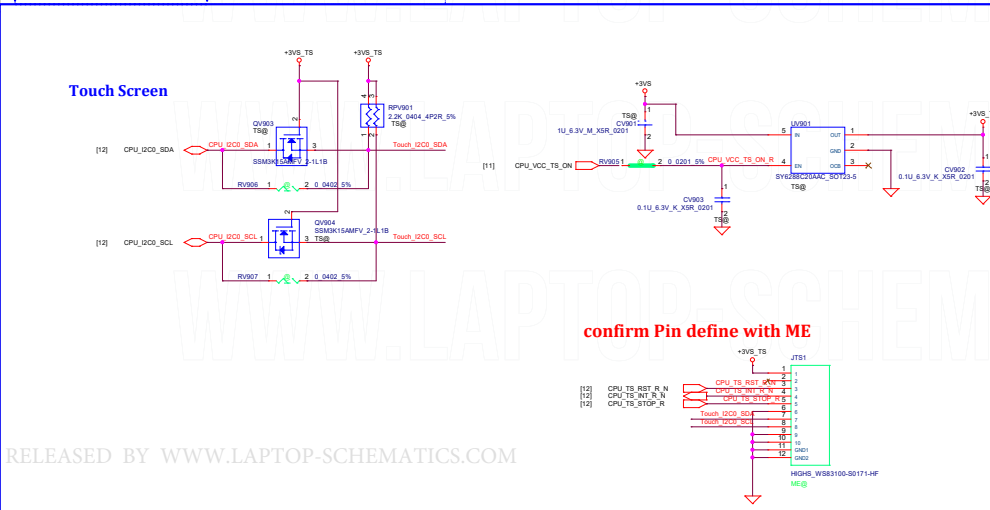
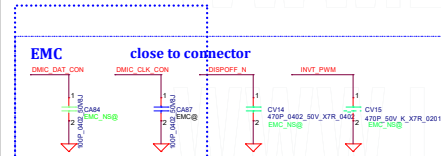
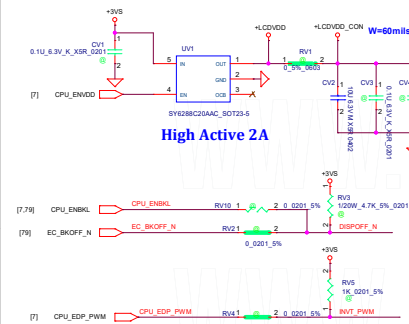
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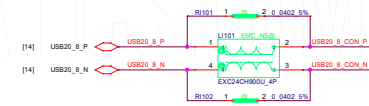
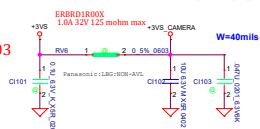
**the different with Base:**

### 1.C970EDP connector pindefine different with S370&V14V15

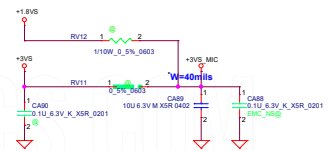


## Camera

FI101 CHANGE TO 00HM 0603

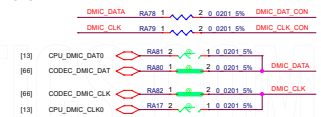


FA1 FA2 CHANGE TO 00HM 0603

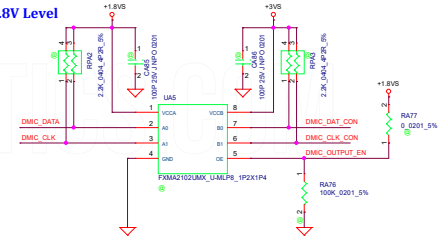


## DMIC

## DMIC 3.3V Level



## DMIC 1.8V Level



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Date:					Friday, March 19, 2022			Sheet 48 of 110

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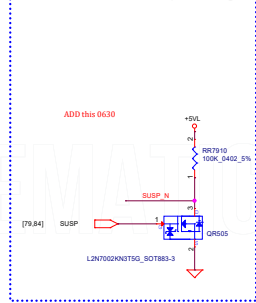
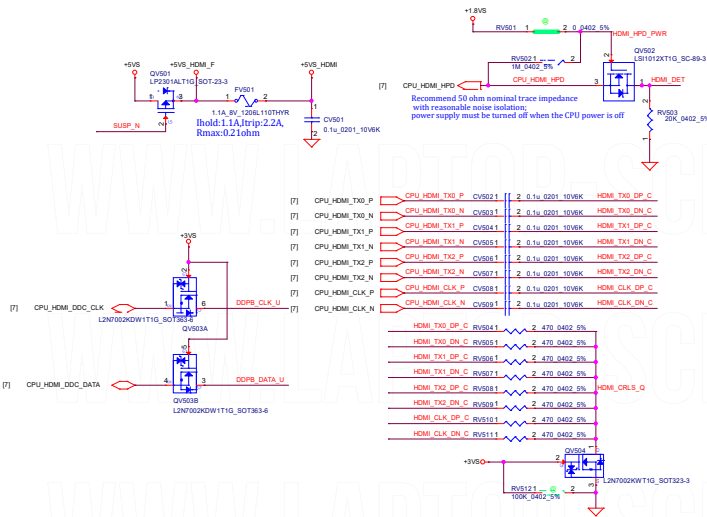
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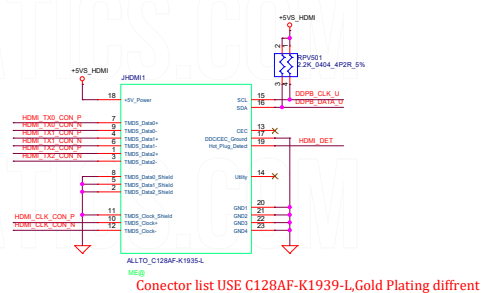
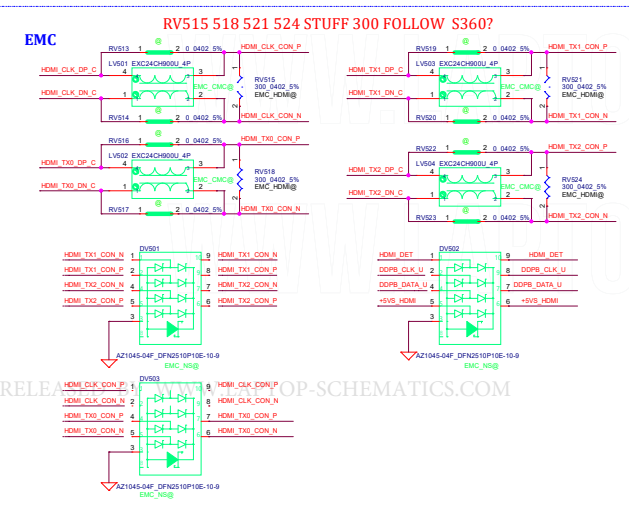
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Date:				Friday, March 19, 2022			Sheet 49 of 110



the diffrent with Base:  
1.C970 No HDMI CONN,\$170 have



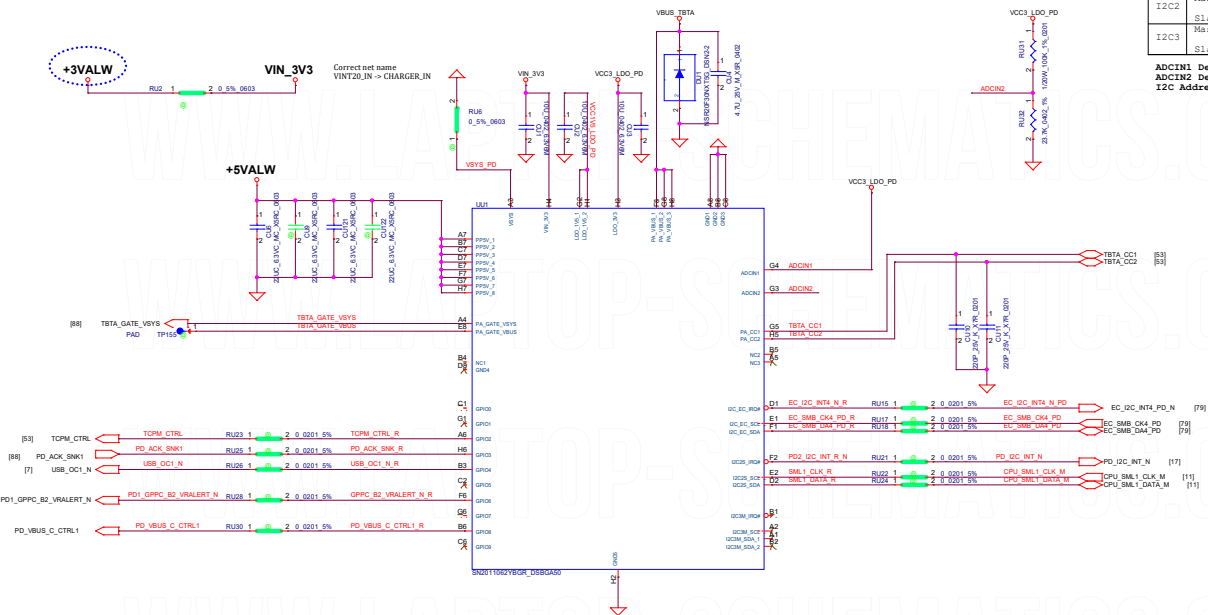
Conector list USE C128AF-K1939-L,Gold Plating diffrent

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Size	C	Document Number	HDMI_CONN	Rev E1
Issue	Friday, March 16, 2012	Sheet	66	of 118

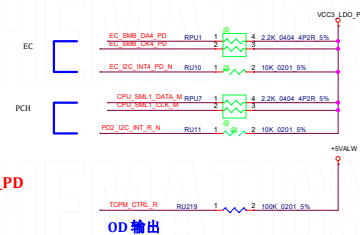
TABLE I2C Addressing

I2C1	Master: EC	TBTA PORT 0x20
	Slave: PD	
I2C2	Master: PMC	TBTA PORT 0x20
	Slave: PD	
I2C3	Master: PD	TBTA PORT 0.B.D.
	Slave: RT	

ADCIN1 Decoded: 7 --tie to LDO\_3V3  
 ADCIN2 Decoded: 4 --0.3022  
 I2C Address Index: 1#



1.S170 have not retimer:  
 remove RU12 RPU2 pull high to VCC3\_LDO\_PD  
 TBT\_I2C\_INT\_N\_R  
 TBT\_I2C\_SCL\_R  
 TBT\_I2C\_SDA\_R



OD 输出

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			Page	Page 19, 2022	Sheet	51 of 118

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				Date:	Friday, March 19, 2022	Sheet 52 of 110	



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				Date:	Friday, March 10, 2022	Sheet	54 of 110

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				Date:	Friday, March 19, 2022	Sheet 55 of 110	

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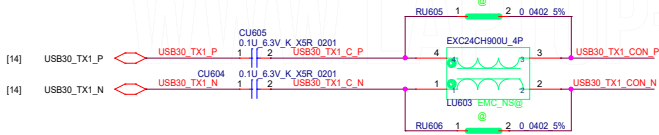
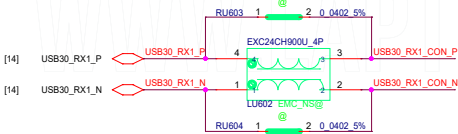
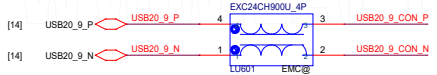
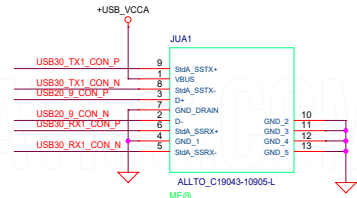
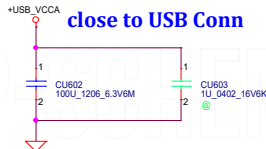
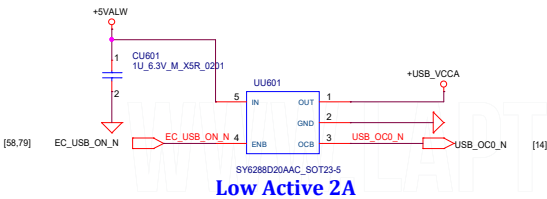
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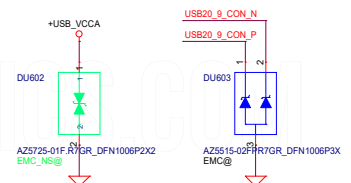
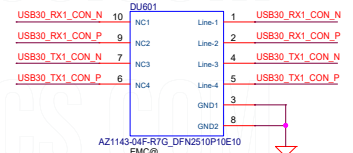
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				Date:	Friday, March 10, 2022	Sheet 56 of 110	

USB3.0 PORT



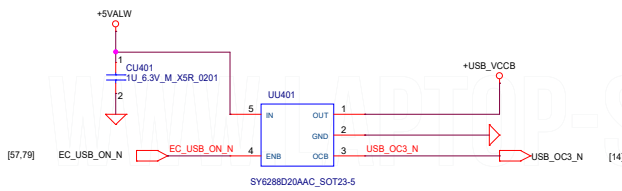
EMC close to USB Conn



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			Date:	Friday, March 19, 2022	Sheet	57 of 110

USB2.0 Port and CMC&TVS&CAP MOVE to SUB Board

USB2.0 PORT



Low Active 2A

the diffrent with Base:  
1.C970 No USB2.0 only,S360&V14V15 have

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				Date:	Friday, March 19, 2022	Sheet	58 of 110

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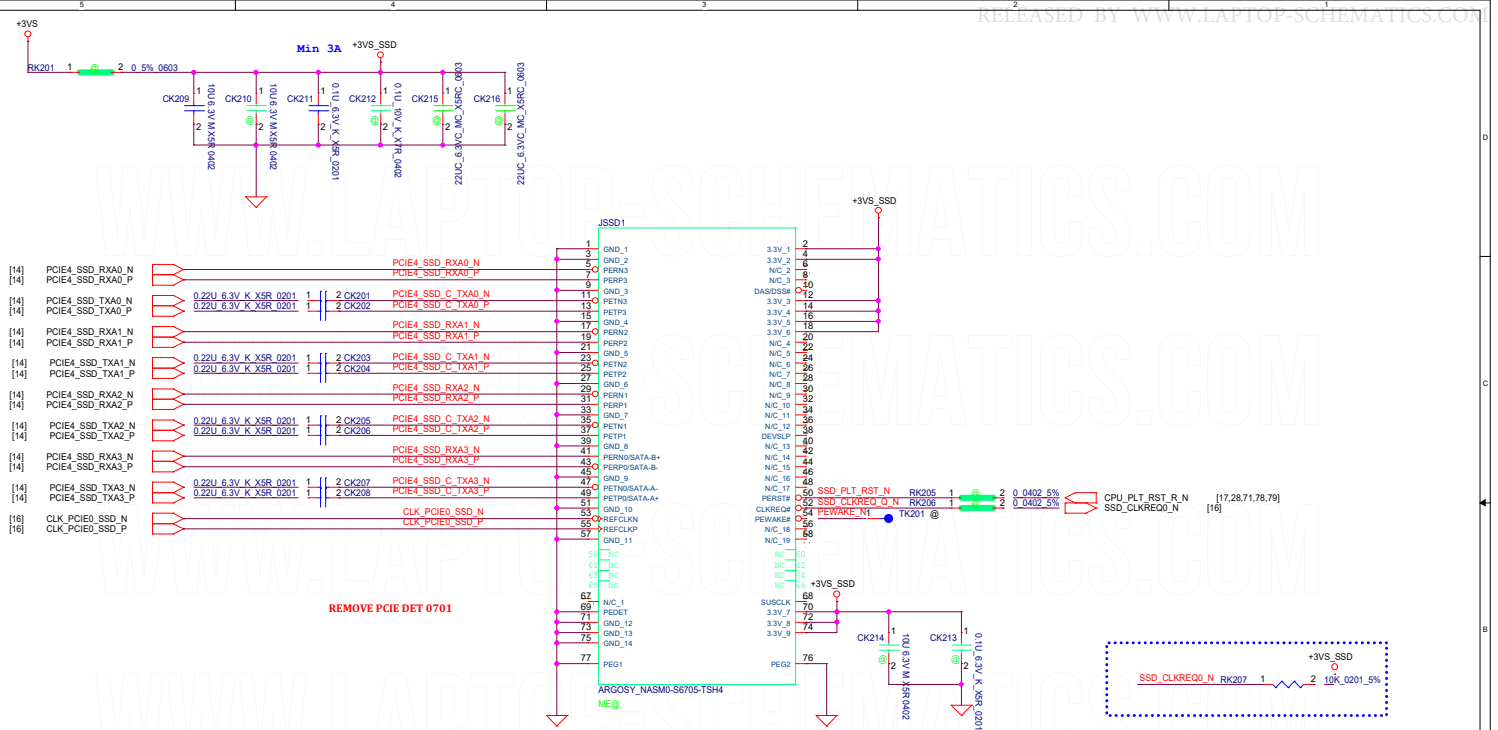
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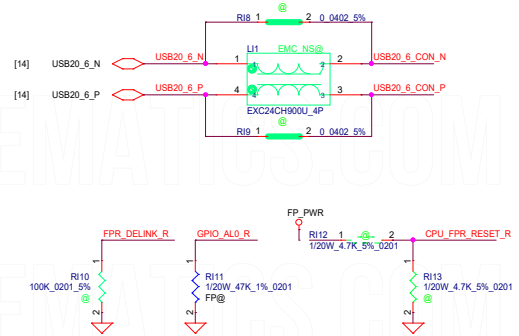
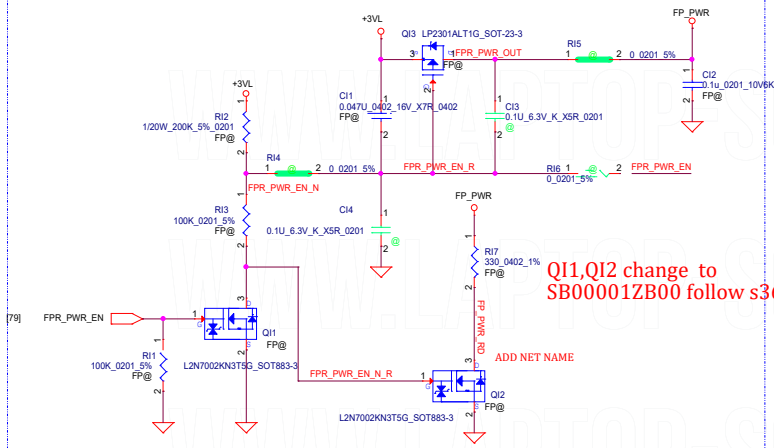
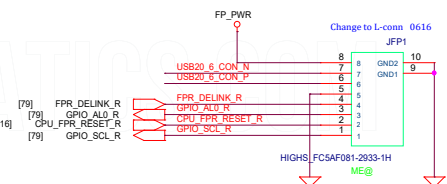
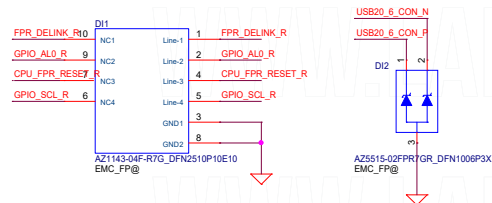
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				Date:	Friday, March 19, 2022	Sheet 64 of 110	

## FP Power Control

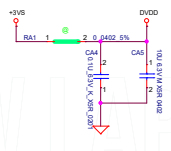
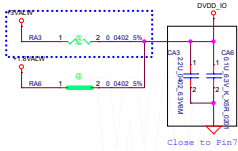
EMC  
close to Conn

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B						Friday, March 18, 2022		J.1	
						Sheet		65 of 110	

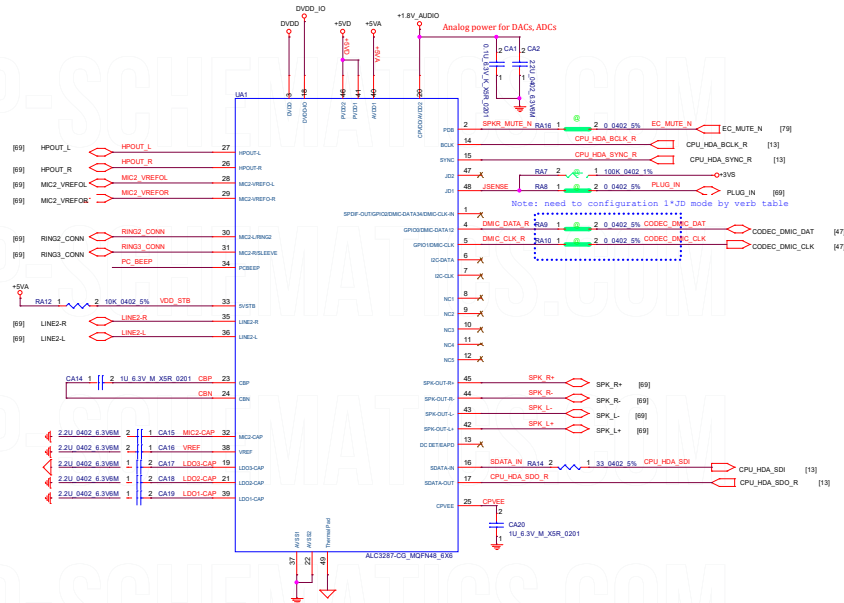
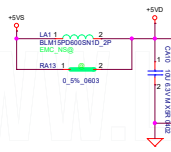
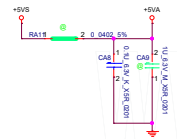
**the different with Base MODULE:**

- 1.Module no ra3 to DVDD\_IO,S360&V14&V15 reserve
- 2.Module no ra5 CA21 to EC\_BEEP,S360&V14&V15 reserve
- 3.RA9&RA10 BOMStructure different with module

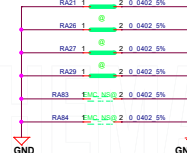
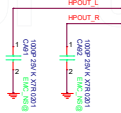
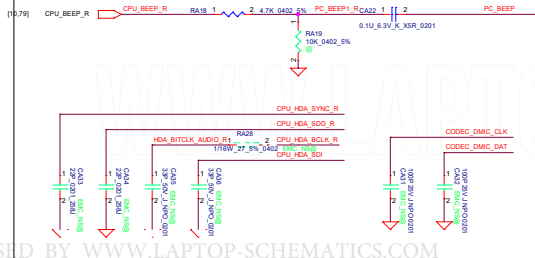
**Note: DVDD-IO must be equal to or smaller than DVDD**



Close to Pin7



Note: power beep function is removed from BIOS spec



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<p>Date Friday, May 10, 2022</p>				Sheet	68 of 110

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				Date:	Friday, March 19, 2022	Sheet 67 of 110	

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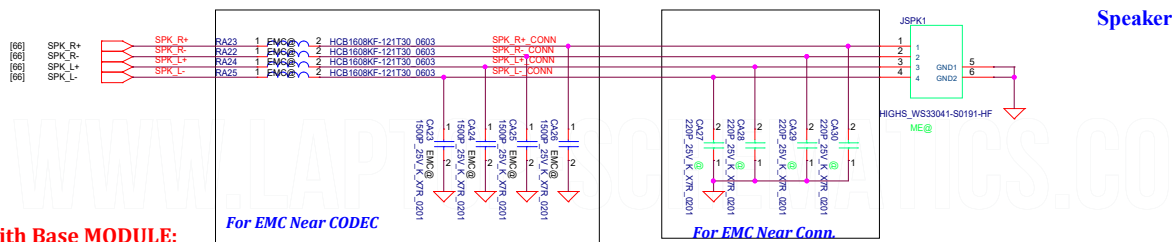
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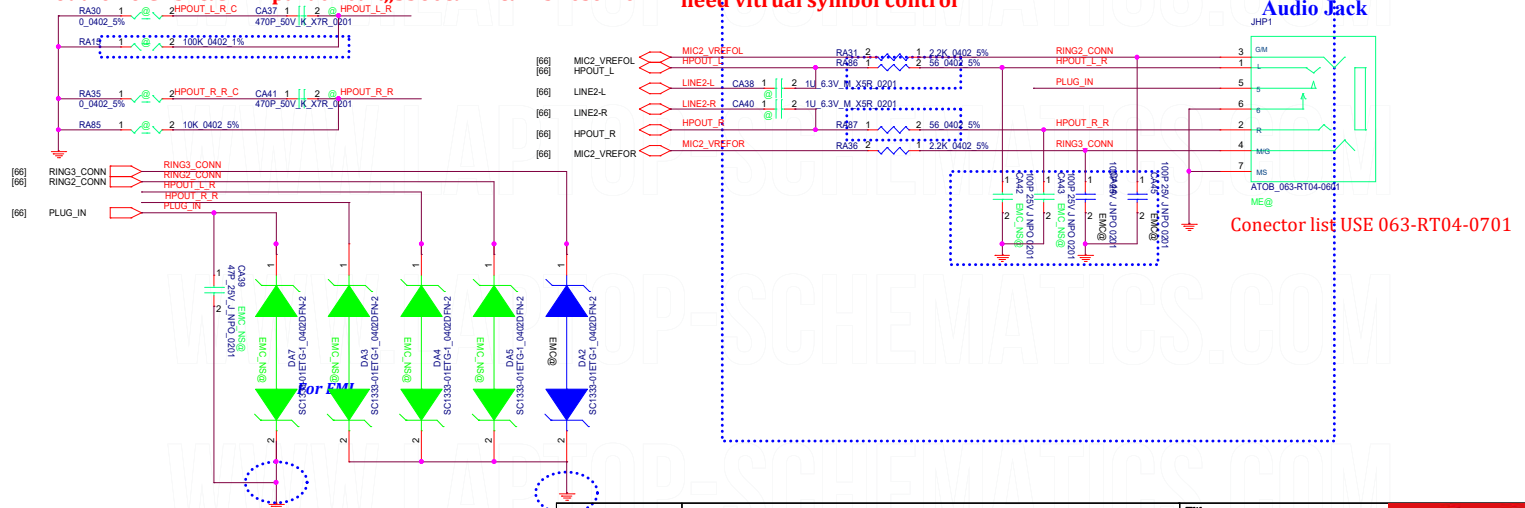
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				Date:	Friday, March 10, 2022	Sheet 68 of 110	



- the different with Base MODULE:
- 1.S360&V14&V15 RA86&RA87 VALUE different with module, Module have RA85&RA88,S360&V14&V15 Remove
  - 2.for EMC TVS EMC\_NS@ type different
  - 3.GND type different
  - 4.module no CA37&CA41 part circuit,S360&V14&V15 reserve

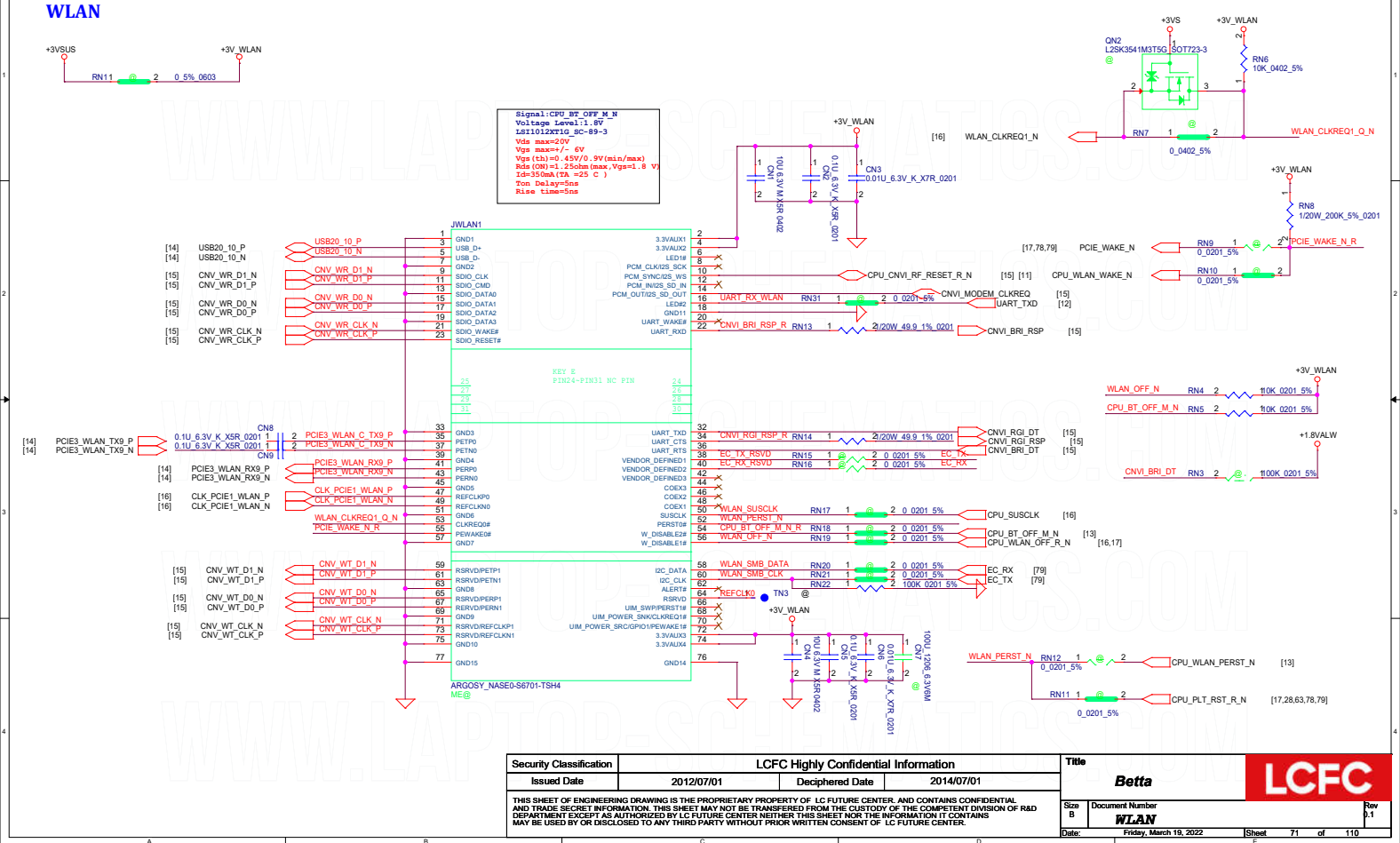


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B		Audio SPK/Jack		Friday, March 10, 2022		Sheet 69 of 110	

Card reader Circuit MOVE to SUB Board S360

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				Date:	Friday, March 19, 2022	Sheet 70 of 110	

## WLAN



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								WLAN	
						Date:		Friday, March 18, 2022	
						Sheet		71 of 110	

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				Date:	Friday, March 19, 2022	Sheet 72 of 110	

LAN Circuit MOVE to SUB Board in V360 DB

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			B	Friday, March 16, 2022		0.1
			Date:	Sheet	73	of 110

LAN Circuit MOVE to SUB Board in V 14 V15 DB

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Date:				Friday, March 19, 2022			
Sheet				74 of 110			

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LAN Circuit MOVE to SUB Board in V360 DB

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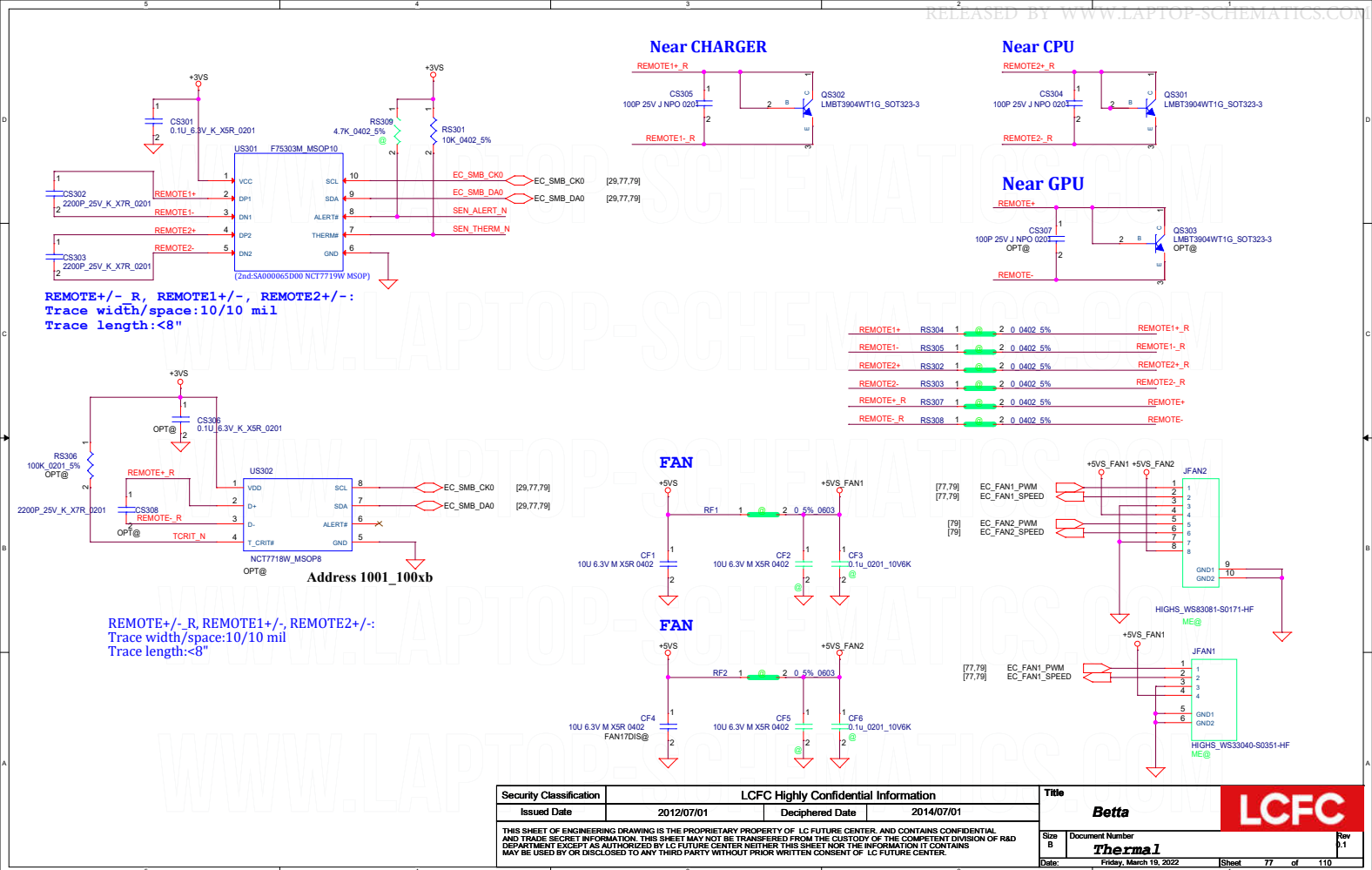
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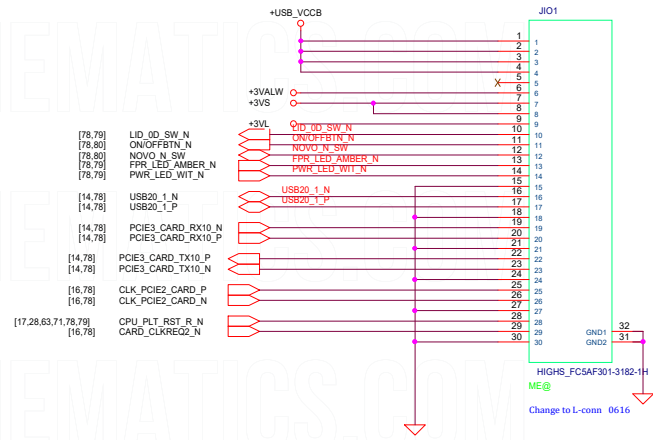
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				Date:	Friday, March 18, 2022	Sheet 76 of 110	



3VALW for LED&V360 Lanchip Power;  
3VS for S360 Card Reader, V360 ISOLATE\_N

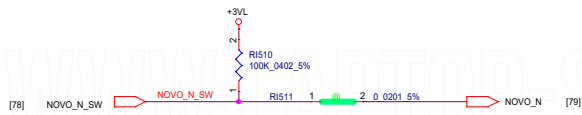
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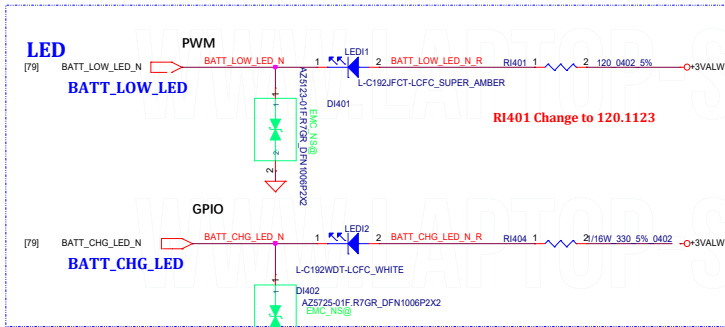
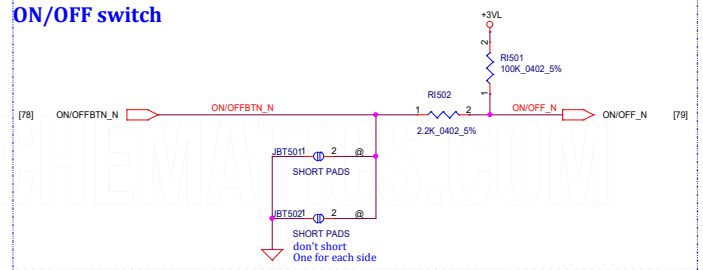
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Document Number		Sub Board CONN		Date		Friday, March 18, 2022		Sheet 78 of 110	
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## NOVO switch



## ON/OFF switch



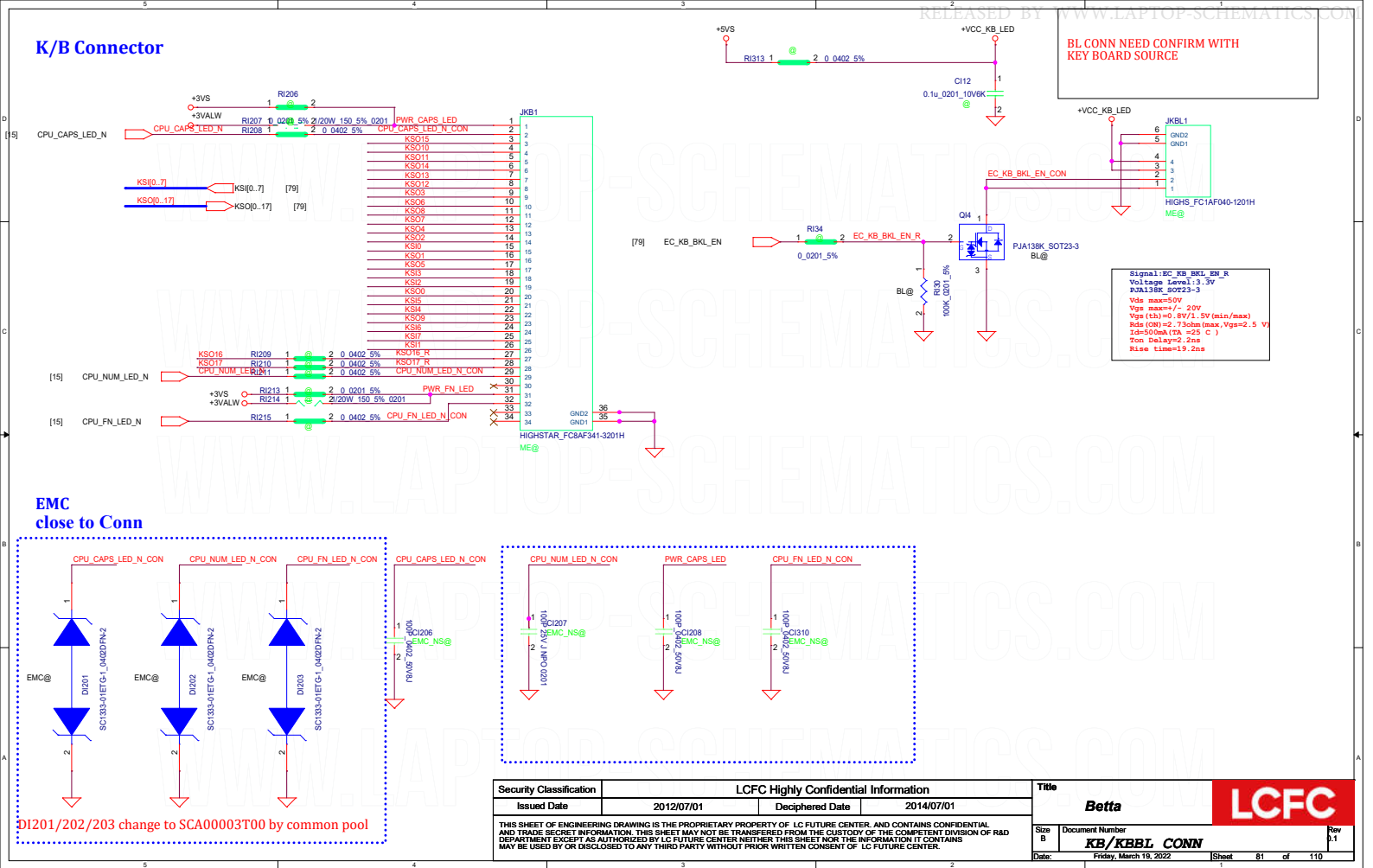
the diffrent with module:  
1.modulel mos control LED,S370&V14V15 NO NEED

LED	Stute	LED Behavior
Power Button	System on	White_on(battery: 21%-100%)
	Standby	White_on(battery: 21%-100%)
	LID closed	Amber_blink_3S(battery: 0%-20%)
	System off	OFF
Charging	Battery only	OFF
	Charging	Amber_on(battery: 1%-90%)
		White_on(battery: 91%-100%)

The Power LED move to SUB board LENS

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Size	Document Number	LED/Button		
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K/B Connector



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				Date:	Friday, March 18, 2022	Sheet 82 of 110	





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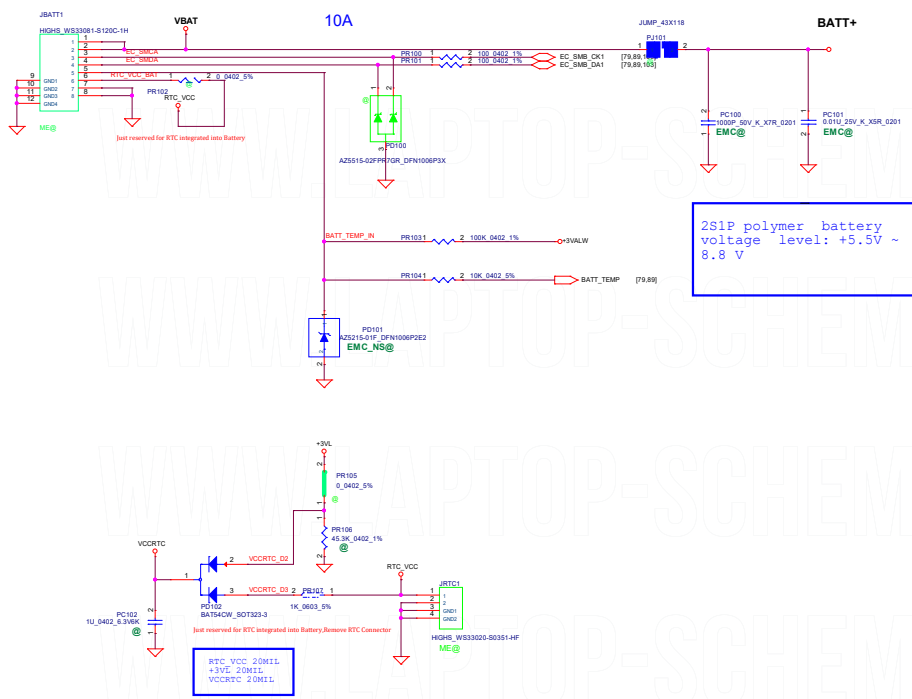
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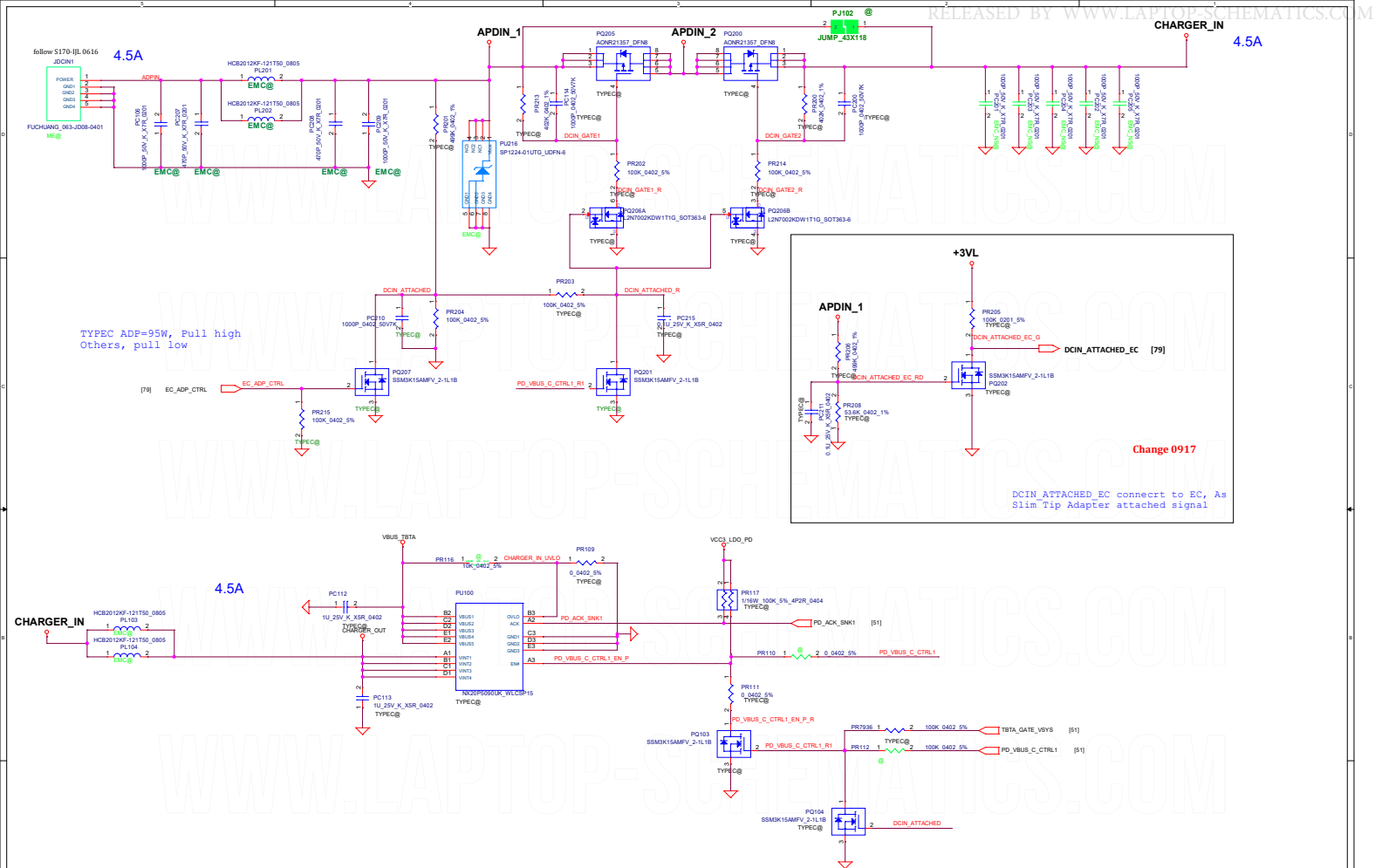
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				Date:	Friday, March 19, 2022	Sheet 85 of 110	




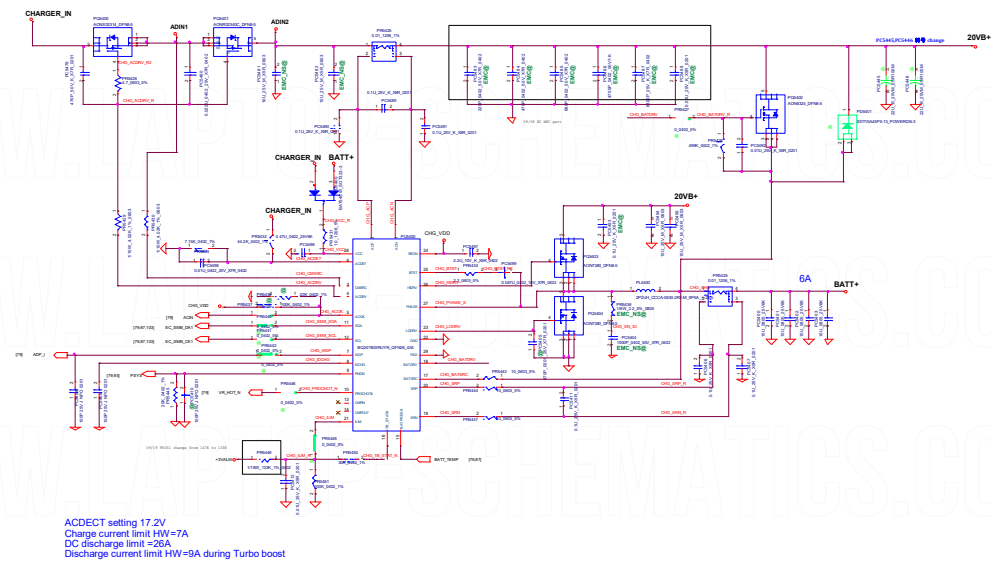


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				PNR DCIN/RTC	
				File	Sheet 87 of 118



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				PHR ACIN	0.1
Date			Sheet		88 of 110



IDPW	V(ILLIM)	PR5320
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K
4.0A	2.6V	162K

V(ILLIM)=1V+40x(VACF-VACN)+1+40x10PR4KAC

← LOGIC


IND IN USE	PR5333
1uH	93K
2.2uH	137K
3.3uH	169K

← LOGIC

# of CELL	VCELL_PRES	PR5322
1-CELL	1.5V	301K
2-CELL	2.4V	150K
3-CELL	3.3V	82K
4-CELL	4.5V	33.2K

← LOGIC

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Revised By	PER CHARGER	Revised By	PER CHARGER	

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	<b>P090-PWR DCC--NA</b>			
<b>Date</b>	2021/01/19	<b>Page</b>	90	of 118

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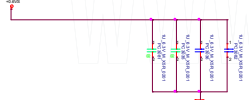
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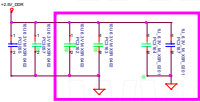


# CHANNELA SLOT DIMM decoupling

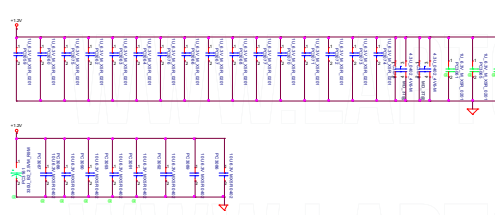
YTT  
PDG 2 Channel SODIMM: 2\*10UF(0603)+4\*1UF(0402)  
S360: channel A:1\*10UF(0402)+2\*1UF(0201)



VPP  
PDG 2 Channel SODIMM: 2\*10UF(0603)+2\*1UF(0402)  
S360: channel A:1\*10UF(0402)+1\*1UF(0201)

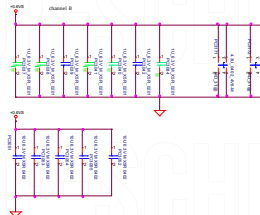


VDDQ  
PDG 2 Channel SODIMM: 1\*330UF(7343)+16\*10UF(0603)+16\*1UF(0402)  
S360: channel A:8\*10UF(0402)+16\*1UF(0201)

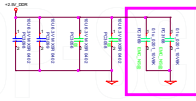


# CHANNELB MD decoupling

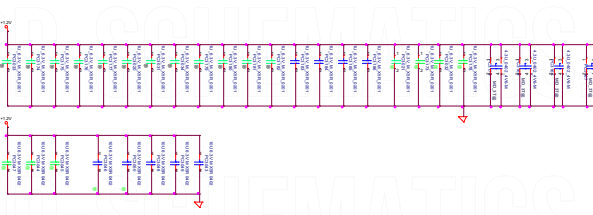
VTT  
PDG 2 Channel MD: 4\*10UF(0603)+16\*1UF(0402)  
S360: channel B:2\*10UF(0402)+2\*1UF(0201)+2\*4.3UF3T(P24)



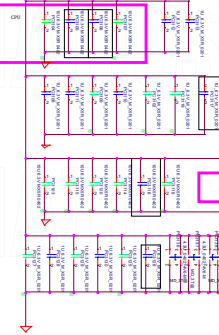
VPP  
PDG 2 Channel MD: 5\*10UF(0603)+16\*1UF(0402)  
S360: channel B:2\*10UF(0402)+8\*1UF(0201)(P26)



VDDQ  
PDG 2 Channel MD: 10\*10UF(0603)+32\*1UF(0402)  
S360: channel B:5\*10UF(0402)+4\*1UF(0201)+3\*4.3UF3T

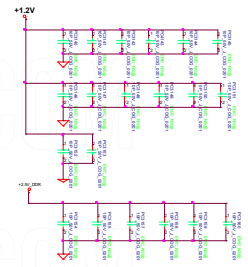


VDD2  
+1.2V PDG: 2\*47UF(0603)+8\*10UF(0402)+8\*1UF(0402)  
S360: 4\*22UF(0603 P93)+4\*10UF(0402)+4\*1UF(0402)

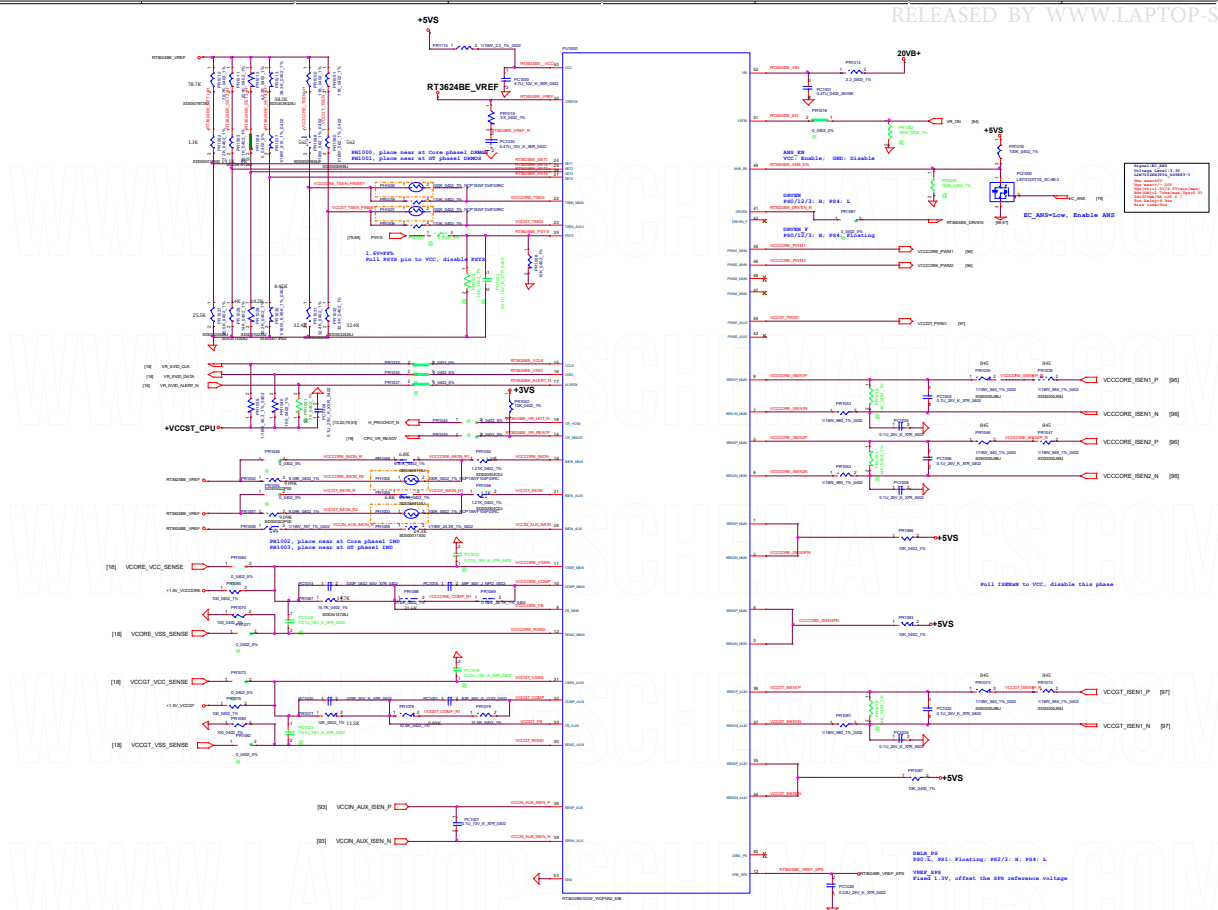


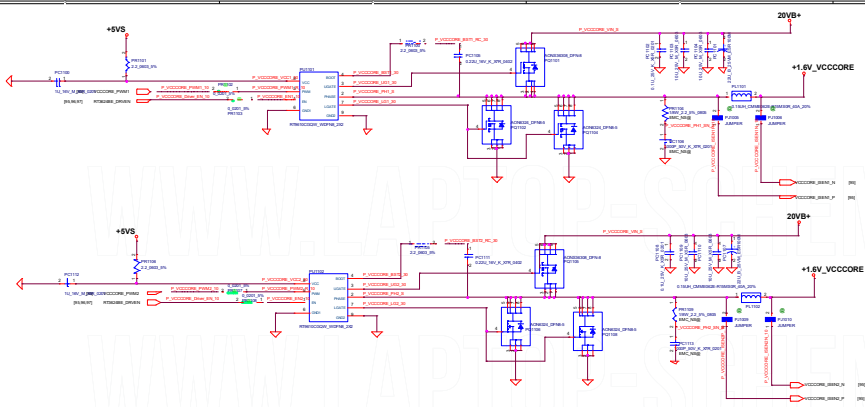
CHANGE VDD2 MLCC 0625

Value	Qty	Note
10u,0402	8	10uF 0402
47u,0603	2	47uF 0603
1u,0402	8	1uF 0402



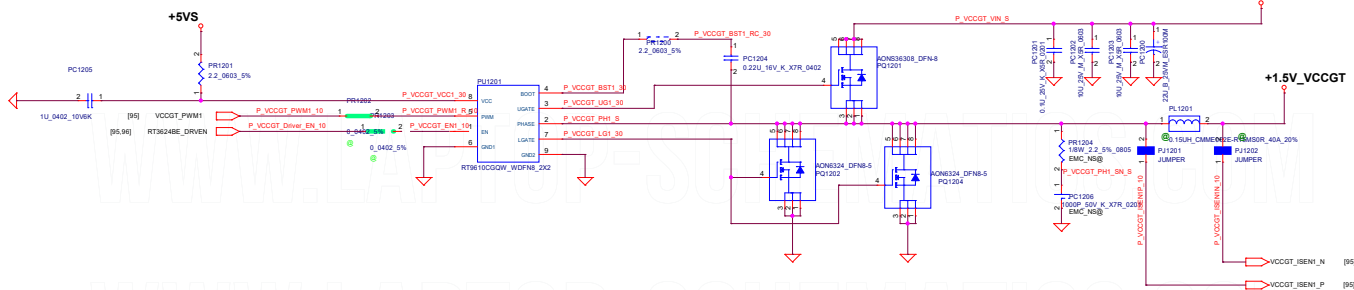
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51	1.5V_VCCCORE
52	1.5V_VCCCORE
53	1.5V_VCCCORE
54	1.5V_VCCCORE
55	1.5V_VCCCORE
56	1.5V_VCCCORE
57	1.5V_VCCCORE
58	1.5V_VCCCORE
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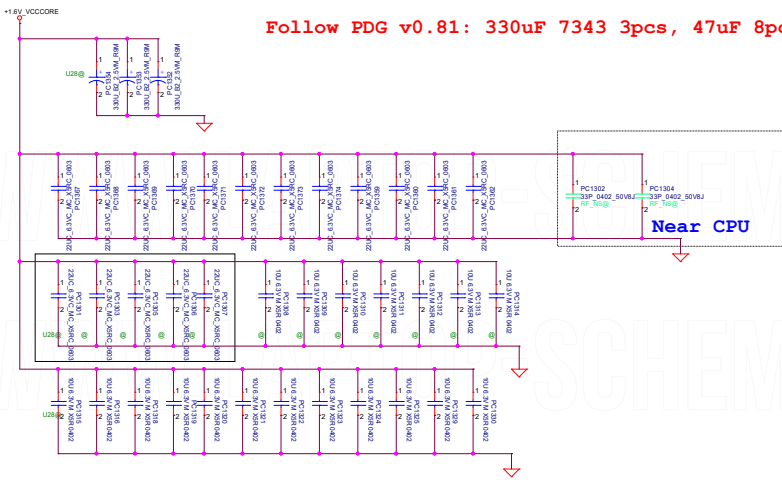
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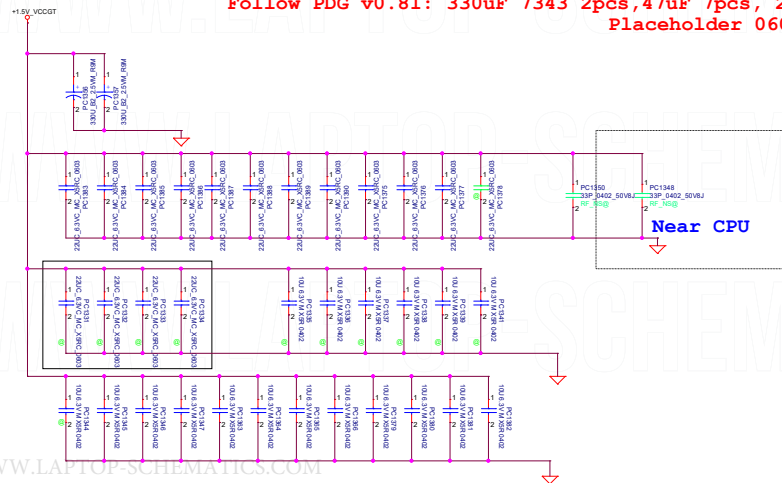
- 1. 5V VCCGT
- 2. 10µF 0.1 5V
- 3. 2.2µF 2.2V 5V
- 4. 0.44µF 0.44V 5V
- 5. 10µF 0.1 5V
- 6. 0.44µF 0.44V 5V
- 7. 10µF 0.1 5V
- 8. 0.44µF 0.44V 5V
- 9. 10µF 0.1 5V
- 10. 0.44µF 0.44V 5V
- 11. 10µF 0.1 5V
- 12. 0.44µF 0.44V 5V
- 13. 10µF 0.1 5V
- 14. 0.44µF 0.44V 5V
- 15. 10µF 0.1 5V
- 16. 0.44µF 0.44V 5V
- 17. 10µF 0.1 5V
- 18. 0.44µF 0.44V 5V
- 19. 10µF 0.1 5V
- 20. 0.44µF 0.44V 5V

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Size	C	Document Number	P097-PWR CPU PWR2	Rev	1.0
Scale	1:1	Drawn	W. 2022	Sheet	97 of 118

Follow PDG v0.81: 330uF 7343 3pcs, 47uF 8pcs, 22uF 8pcs



Follow PDG v0.81: 330uF 7343 2pcs, 47uF 7pcs, 22uF 8pcs, 10uF 2pcs  
Placeholder 0603\*1, 0402\*2



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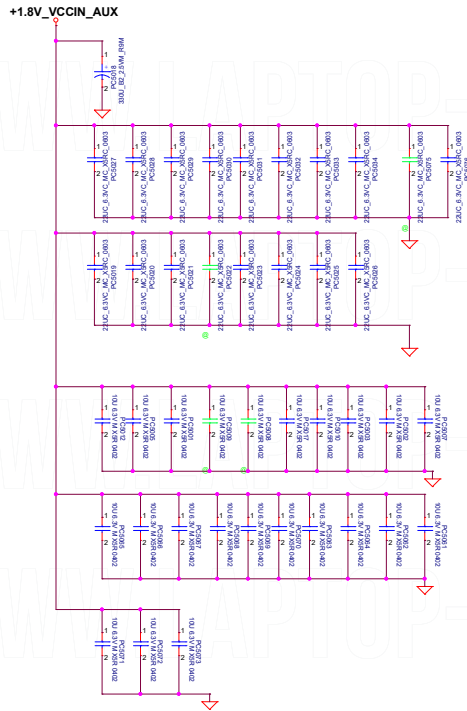
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				C	1.0
Document Number				P100-PWR PCH PWR2	
Date				Friday, March 10, 2023	
Sheet				100 of 110	

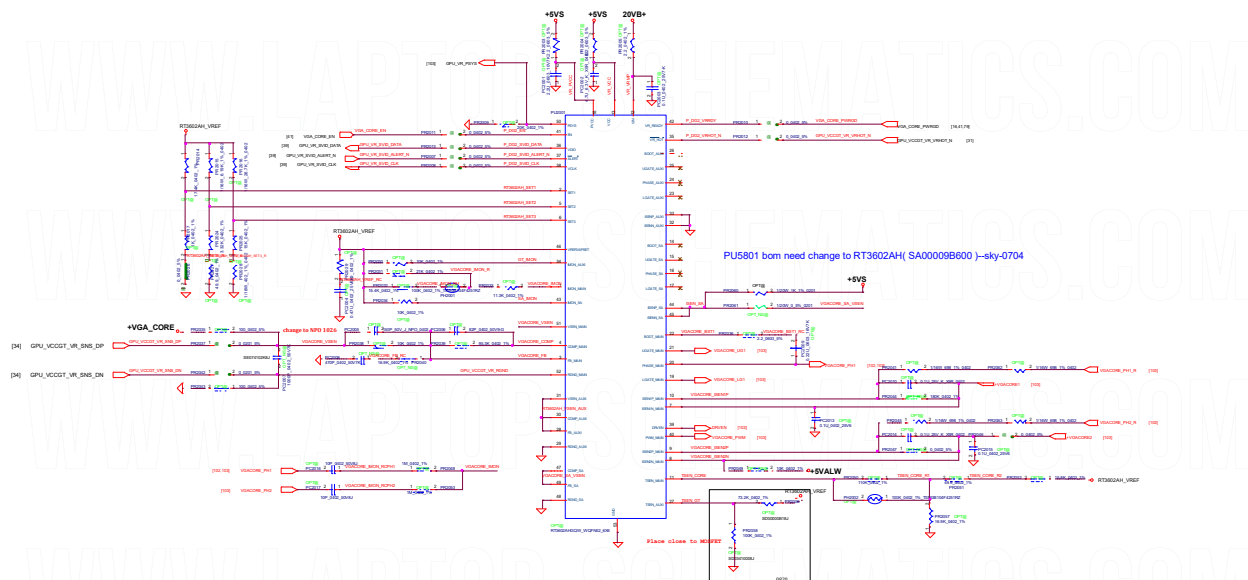
Follow PDG v0.81:330uF 7343 1pcs, CPU side 47uF\*8, 10uF 10pcs



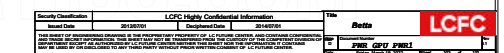
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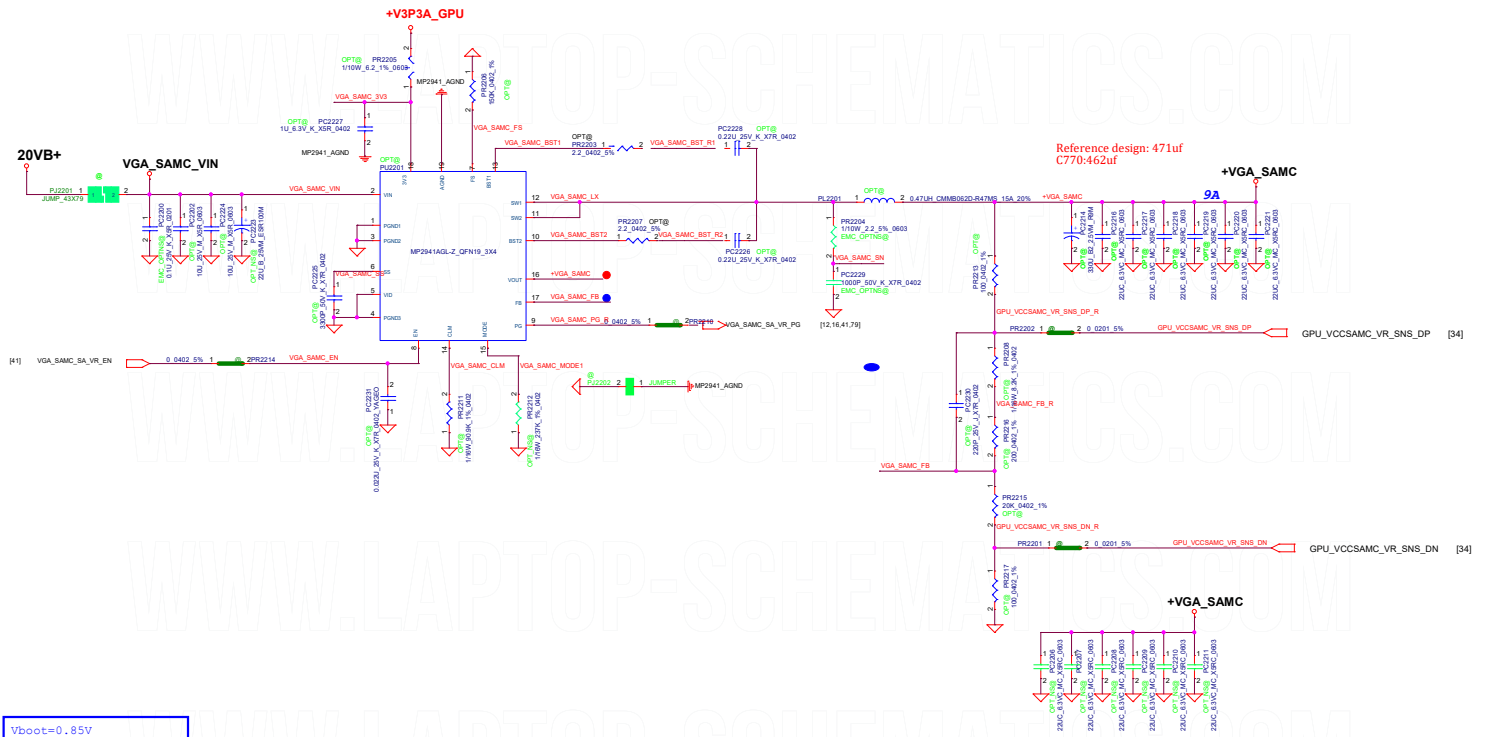
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				Docuement Number	LCFC
				P101-PWR PCH PWR Decoupling	
				File	Sheet 101 of 118

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Issue Date	2010/07/01	Issued Date	2010/07/01	
Part Name				LCFC
Part Description				PMU GPU PMU Controller





Vboot=0.85V  
Ripple=+3.5/-5%  
TDC=9.3A Iccmax=14.3A  
OCP=14A  
Vref=0.7V  
OVP=(1.2~1.3)\*Vref  
UVP=(0.65~0.75)\*Vref  
Fsw=400Khz

VGA\_SA  
Vboot=0.85V  
Ripple=+3.5/-5%  
TDC=4.5A Iccmax=6.2A  
OCP=25A

VGA\_SAMC  
Vboot=0.85V  
Ripple=±25mV  
TDC=4.8A Iccmax=8.1A  
OCP=25A

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Doc No	PWR GPU PWR2			Issue	1.1
Date	Friday, March 19, 2022			Issue	1.1

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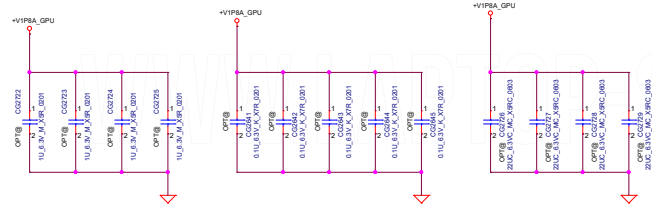
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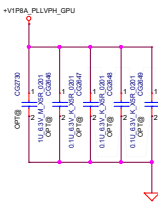
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Size		C		Document Number		P105-PWR GPU PWR Monitor-NA		Rev	
Scale		1:1		Title		P105-PWR GPU PWR Monitor-NA		Rev	
				Date		Friday, March 10, 2012		Sheet 106 of 113	

## +V1P8A\_GPU RAIL



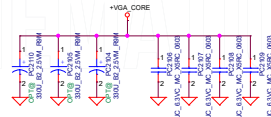
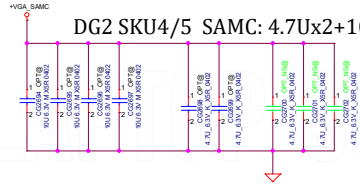
## +V1P8A\_PLLVPH RAIL



GPU DECOUPLING: VCCSAMC\_GPU

SECONDARY SIDE  
TO BE PLACED CLOSE THE GPU

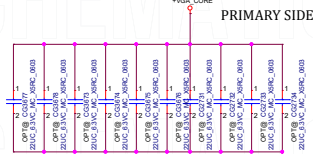
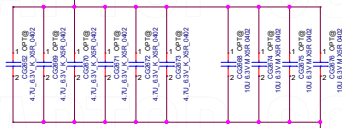
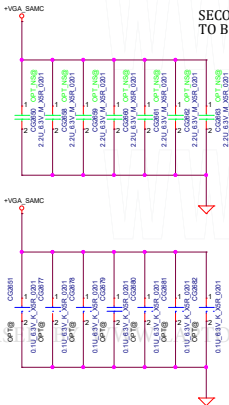
DG2 SKU4/5 SAMC: 4.7Ux2+10Ux4



TO BE PLACED NEAR THE VREG

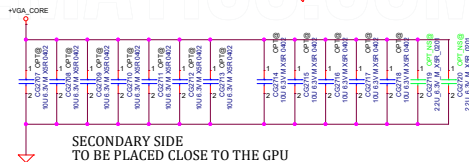
SECONDARY SIDE  
TO BE PLACED CLOSE THE GPU

DG2 SKU4/5 SA: 4.7Ux6+10Ux4



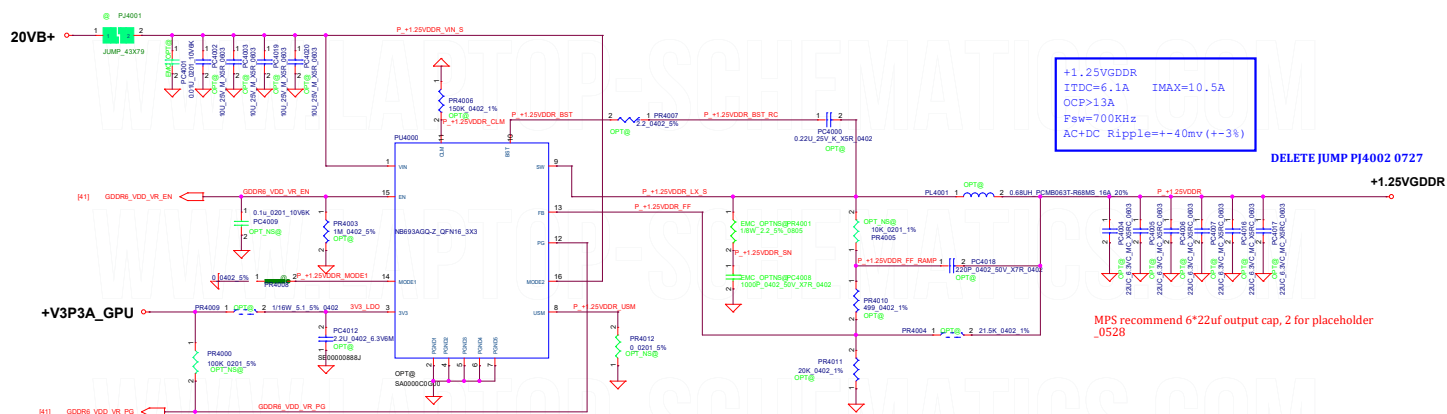
PLACEHOLDER (FOR SOCKET COMPENSATION)

Follow AEP



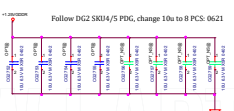
SECONDARY SIDE  
TO BE PLACED CLOSE TO THE GPU

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Size	C	Document Number	P106-PWR GPU PWR Monitor-NA	Rev	1.1
Issue	1	Issue Date	March 10, 2022	Sheet	106 of 113

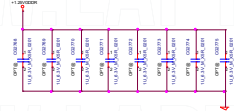


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			Date	PWR VZAM PWR	107	1
			Date	Mar 26, 2022	Sheet	107 of 113

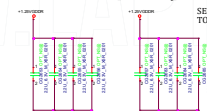
Follow DG2 SKU4/5 PDG, change 10u to 8 PCS: 0621



4 CAPS PER DRAM, 2 CAP PER EDGE/QUADRANT WITH VCCDDRQ BGAS



GPU DECOUPLING: VCCDDR\_GPU VCCDDQ\_GPU



SECONDARY SIDE  
TO BE PLACED CLOSE TO GPU

Change 2.2u to 4.7u

two 10uf\_two 4.7u\_0621

[illegible]

Change List

- 1.RC265 change to 0201 for ME request
- 2.ADD RG4155 for DGPU\_PERTST\_N shutdown glitch, RG3855 no stuff
- 3.RC188, RC169 change to 0201/1%
- 4.PC7925(0.22U) change to CG7925(0.01U), PC7927(0.22U) change to CG7927(0.01U)
- CG2631 change to 0.022U, RG2694 change to 0ohm
- 5.RG4147 change to 10K, ADD RG4154, ADD DG1000
- ADD RG4156
- 6.ADD RU120, RU121, RU122, RU123 FOR S170
- 7.RC314 no stuff
- 8.RU32 change to 23.7K, DELETE CU7, CU8, CU121 stuff
- 9.delete UG7, RG121 RG4138, ADD CG927, DG231, QG3529, QG3530, RG121, RG4138, RG4157
- 11/22
- 1. GPP\_E22, ADD 10K PULL DOWN RSVD
- 11/23
- 1.RI206, RI213 Change to 0ohm
- 12/06
- 1.P28, PEG\_RST\_N pull high to V3P3AGPU, PEG\_RST\_M1\_N pull high to 1.8VALW\_PCH
- 2.RI101, RI102 change to 0ohm

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Change List 22				

1. del PR2059

2022/02/08

2.ADD PC5075,PC5076

1.PJ2201 Change to PL2202

3.GPU PWR conntroller VCC PVCC change to +5VS,PR2060 stuff,PR2061 no stuff

4.DCIN\_ATTACHED\_EC change to pull high to +3VL ,PQ202 SWAP,PR206 change to 499K

5.PR2214 change to 0 ohm

6.ADD PC2110, ADD PR2062,PR2063,PR2041 ,PR2045change to 698ohm

7.PR2031 change to 23.7K,PR2032 change to 12.7K

PR2033 change to 16.9K,PR1068 change to 31.6K

PR1069 change to 26.7K,PC1015 change to 56PF

PR1078 change to 10.5K,PR2039 change to 30.1K

PR2056 change to 73.2K,PR2058 change to 100K

CG2717,CG2718,CG3671,CG3672 stuff

8.CPU power电感换2.4mm高的sample: PL1101,PL1102,PL1201,PL1501并增加相应的short pin

9.非core power的电感主料换Coilforce的PN(PL6502,PL3001,PL5701,PL5400,PL5601)

10.PQ 1102,PQ1104,PQ1106,PQ1108,PQ1202,PQ1204,PQ1502 change to AON6324

11/23

1.PR2033 16.9K change to 11.3K

PR2031 23.7K change to 21K

PR2032 12.7K change to 15.4K

PR2039 30.1K change to 95.3K

PC2005 220P change to 150pF

PR2028 470 change to 402R

PR2015 2.37K change to 6.19K

PR2024 1K change to 3.32K

PR2027 442 change to 49.9R

11/25

1.PC2202,PC2224,PC4002,PC4003,PC4019,PC4020,

PC5494,PC5495,PC5601,PC5604,PC5703,PC5704

change to SE000010U00

2.Delete PJ1501,PJ1100,PJ1101,PJ1200 ,delete PD2000

12/13

1.P103: delete PJ2101,ADD PR2130,PR2131,ADD PU2102及其周边相关电阻 电容,

2.P104: 20VB+ change to 20VB+\_GPU

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				Date: Friday, March 18, 2022	Sheet 110 of 110